LOW POWER ENCODER AND COMPARATOR DESIGN OF 5-BIT FLASH ADC

YATISH LAVANIA

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI DESIGN AND EMBEDDED SYSTEM

By

Yatish Lavania

Department of Electronics and Communication Engineering

National Institute Of Technology

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Under the Guidance of
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To my parents.

NATIONAL INSTITUTE OF TECHNOLOGY

ROURKELA

CERTIFICATE

This is to certify that the thesis titled **"LOW POWER ENCODER AND COMPARATOR DESIGN OF 5-BIT FLASH ADC"** submitted by **Mr. YATISH LAVANIA** in partial fulfillment of the requirements for the award of Master of Technology degree in **Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded System**" during session 2011-2013 at **National Institute Of Technology, Rourkela** is an authentic work by him under my supervision and guidance.

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Yatish Lavania

Abstract

The present work of the thesis is divided into two parts, first is design of a low power encoder and second is low power latched comparator design. In this low power encoding scheme proposed for 4GS/s 5 bit flash analog to digital converter. The demanding issues in the design of a low power flash ADC is the design of thermometer code to binary code. An encoder in this thesis converts the thermometer code into binary code without any intermediate stage using dynamic CMOS logic. To decrease the power consumption of the Flash ADC, the implementation of encoder and comparator is done using dynamic CMOS logic. The proposed encoder in this thesis is designed using 90nm technology at 1.2V DC voltage source using CADENCE tool. The simulation results of 5-bit Flash ADC block is shown for a sampling frequency up to 4GHz and at 4GHz the encoder circuit showing the average power dissipation of the encoder block is 1.833 µW.

The other part of the present work is the design of low power comparator for the 5-bit flash ADC. Dynamic latch comparator has been designed in order to reduce power dissipation, delays etc. The different parts of the dynamic latch comparator like: pre-amplifier, dynamic latch, and output buffer are implemented on CADENCE tool with 1.2 V power supply. The simulation results shown for a sampling frequency of 5 GHz and the average power dissipation of the proposed comparator is 69.09 µW. The physical layout of the encoder and comparator has been drawn using CADENCE VIRTUSO LAYOUT EDITOR. The DRC errors has been removed and the layout has been matched with the schematics.

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Introduction

The signals in the real world are analog in nature for example light, sound, video etc. In order to achieve digital signal, we need to convert the analog signal into digital form by using a circuit called analog-to-digital converter. Whenever we need the analog signal back, digital-to-analog converter is required. Analog to digital converters are vital to many modern systems that require the integration of analog signals with digital systems. The applications of digital system can range from audio to communications applications to medical applications. These converters are implemented using a variety of architectures, sizes and speeds. The demand for the converter is oriented on area, speed, power of the converters. This has led to the investigation of alternative ADC design techniques.

Most modern digital systems consist of multiple integrated circuits (ICs), which need to communicate with each other. As the processing speed of each IC increases, it demands higher and higher input/output (I/O) bandwidth. The term high-speed link refers to both the physical channel and the I/O circuits that goal is to support this increasing need for bandwidth. To keep up, high-speed links are forced to both employ more parallel channels and increase the data rate in each channel.

1.1 Motivation:

Analog-to-digital converters (ADCs) are used to convert real world analog signals into digital representations of those signals. As we know that the digital signal processing can then efficiently extract information from the signals. ADCs find use in communications, audio, sensors, video and many other applications. High-speed (multi-GHz sampling rate), low-resolution (4- to 8-bit) ADCs are used in oscilloscopes, digital high-speed wireline and wireless communications and radar. Flash and time-interleaved ADCs architectures are typically used for high-speed applications. There are various type ADC architecture in which first is pipeline ADC. Its operating speed is high but below flash with medium resolution. Second ADC architecture is SAR ADC. It is Suitable for low power and medium-to-high resolution applications with moderate speed. Third ADC architecture is Sigma-delta ADC. It is suitable for high resolution and low speed applications. Forth ADC architecture is Flash ADC. It can Operates at high speed and low resolution.

So we can say that Flash ADC is the fastest ADC in comparison with other ADC architectures. The flash ADC is the best choice in high speed low resolution applications. it is highly used in high data rate links, high speed instrumentation, radar, digital oscilloscopes and optical communications. Since flash ADC is operating in parallel conversion method, maximum operating frequency in the range of gigahertz is possible.

Comparator design is also a challenge for design of 5-bit Flash ADCs. Here we use the Dynamic Latched Comparator in the comparator block. Latches and flip-flips can be static or dynamic. A dynamic latch or flip-flop gradually loses its content as time goes, while a static one retains its content no matter how much time is elapsed. The charge will leak out of the output capacitor of the dynamic latch as time goes and thus the content of the latch is lost. So the use of a dynamic latch should be carefully scrutinized.

1.2 Problem Description:

It is possible to use conventional ADC architectures, such as FLASH or interleaved pipeline or successive-approximation ADCs, for the link receiver front-ends. Unfortunately, neither of these ADCs is very efficient for the range of resolution and conversion rates typically needed for high-end link receivers. Therefore, in this work, we attempt to find a different ADC architecture that would directly exploit the specificity of a high-speed link environment to provide much better power- and area-efficiency. In particular, the availability of precise and very fine timing references present in high-speed links hints at better exploiting the time dimension. To this end, we propose an interleaved single-slope ADC that can be thought of as a time-domain equivalent of FLASH, only with smaller input capacitance, good intrinsic linearity, and low power consumption. With this example, we hope to demonstrate that the advantages of developing novel circuits, possibly very unconventional, but with their architecture driven by the specific needs of the overall system, can far outweigh additional difficulties and risks associated with the development.

Power dissipation is one the most important concerns in ADCs used for battery operated devices. It is important to track the trends in ADC power efficiency during the past years.

1.3 Thesis Organisation:

This thesis provides a Low Power Encoder and Comparator Design of 5-bit Flash ADC. Simulation results gives High Speed, less offset, low power dissipation, low noise. Thesis can be organized in the following manner.

Chapter 2 focuses on Basics of Analog–To-Digital Converter (ADC), Different architectures of ADCs are studied in this section along with advantages and disadvantages of the different ADC architecture. At the end of this chapter the comparison of different ADC architectures is presented with respect to their resolution, conversion time, area etc.

Chapter 3 focuses on the ADC Characterization in which

Chapter 4 focuses on Design of Flash ADC using dynamic CMOS logic in which the architecture of resistor ladder, comparator and decoder block of flash ADC. In this chapter best fit architecture of comparator block is described and architectures of decoder block have been discussed.

Chapter 5 focuses on implementation of flash ADC in 90nm using Cadence Tool.

The all results (including experimental values) of different blocks of 5-bit Flash ADC are shown in table.

CHAPTER 2
ADC ARCHITECTURES

INTRODUCTION

ADC ARCHITECTURES

ADC COMPARISON

ADC Architectures

Analog to digital converters are the basic building blocks that provide an interface between an analog world and the digital domain. As it is the main block in mixed signal applications, it becomes a bottleneck problem in data processing applications and limits the performance of the overall system. In this chapter we will give the introduction of a number of A/D converter architectures. We will start from the basic definition of ADC then we will look into different architecture of ADCs that include Flash, Successive Approximation (SAR), Sigma-Delta, Pipeline and Dual Slope ADCs. At last we will compare the different architectures and will see the impact of CMOS technology on ADC architectures.

2.1 Introduction:

Analog to Digital Converter (ADC) is a device that accepts an analog value (voltage/current) and converts it into digital form that can be processed by a microprocessor. Figure 2.1 shows a simple ADC with analog input and digital output bits.

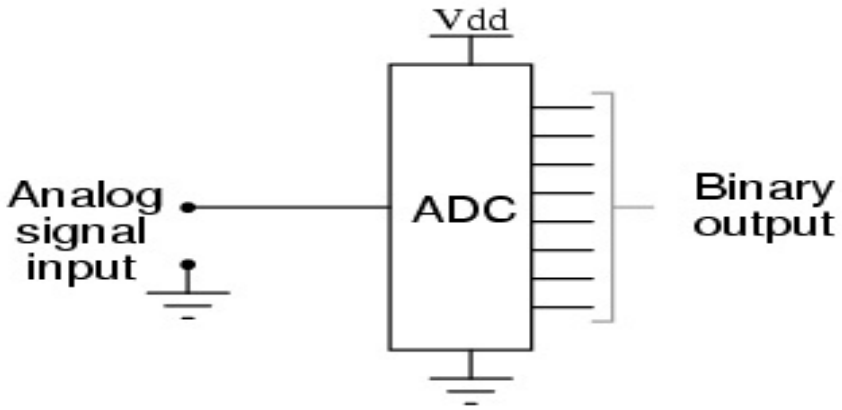


Figure 2.1. Block Diagram of ADC

2.2 ADC Architectures:

There are number of architectures available to develop an ADC that depends upon speed, accuracy, resolution etc. The most common types of ADCs are pipeline, successive approximation, dual slope and sigma-delta, flash.

2.2.1 Flash ADC:

Flash ADC's are also called parallel ADCs. Due to the parallel architecture it is the fastest ADC among all the other types and are suitable for high bandwidth applications. Due to presence of 2^N resistor it consumes a lot of power, has low resolution, and expensive for high resolution. It is mainly used in high frequency applications and in the other types of ADC architectures e.g. multi bit sigma delta and pipelined. Few applications of flash ADCs are satellite communication, radar processing, data acquisition, sampling oscilloscopes, and high-density disk drives. A typical flash ADC block diagram is shown in figure 2.2.

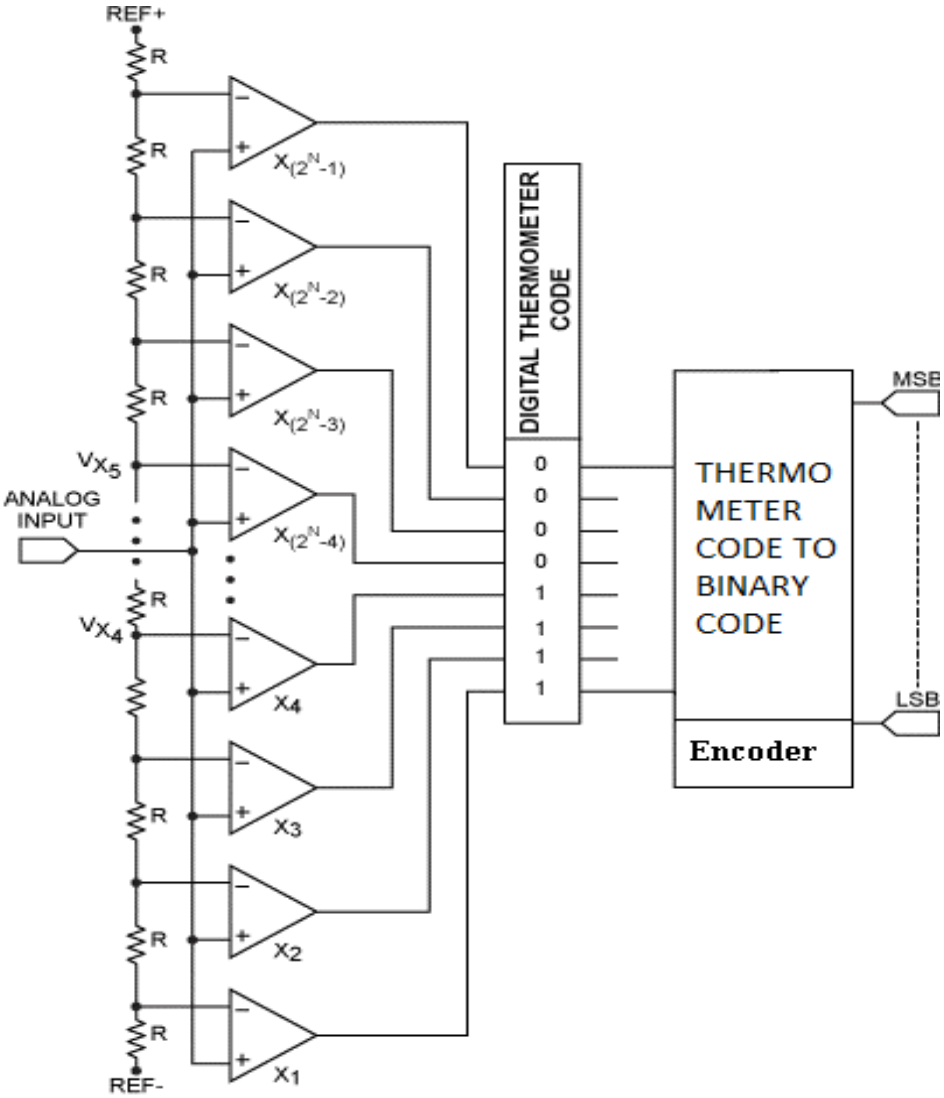


Figure 2.2: Block Diagram of Flash ADC [4].

It can be seen from the figure 2.2, that $2^N - 1$ comparators are required for an "N" bit converter. The resistor ladder network is formed by 2^N resistors, which is used to generates the +reference voltages for the each comparators. The reference voltage for each comparator is 1 least significant bit (LSB) less than the reference voltage for the comparator immediately above it. When the input voltage (positive terminal) is higher than the reference voltage (negative voltage) of comparator it will generate a "1", otherwise, the comparator output is "0". If the analog input is in between Vx_4 and Vx_5 , then the comparators X_1 through X_4 generates "1"s and all the remaining comparators generate "0"s.

The comparators will generate a thermometer code of an input signal. This code is known as thermometer code, because it is similar as mercury thermometer, where in the mercury column, the mercury always rises to the appropriate temperature and no mercury is present above that temperature. This thermometer code will then encode into a binary form by thermometer-to-binary encoder. They are typically low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. They are designed to obtain the low offset voltage, such that the condition of the comparator is that its input offset of each comparator is smaller than 1 LSB of the ADC. Otherwise, the offset of the comparator could falsely trip the comparator output, due to this the digital code at the output of comparator block is not a representative of a thermometer code. A regenerative latch present at each comparator output stores the result. Due to presence of positive feedback, the end state is forced to either a "1" or a "0".

2.3.2 Sigma-Delta ADC:

Figure 2.3 shows a sigma-delta ADC that uses a 1-bit DAC, filtering, and over sampling to achieve very accurate conversions. Low frequency signal is applied to the input of a sigma-delta ADC. 1 Bit DAC will quantize this input signal at high frequency. The digital decimator filter will reduce the sampling rate and increase ADC resolution. E.g. if the sampling frequency was 4MHz then the oversampling will reduce the sampling rate to about 16kHz and increases the ADC's resolution (i.e., dynamic range) to 16 bits.

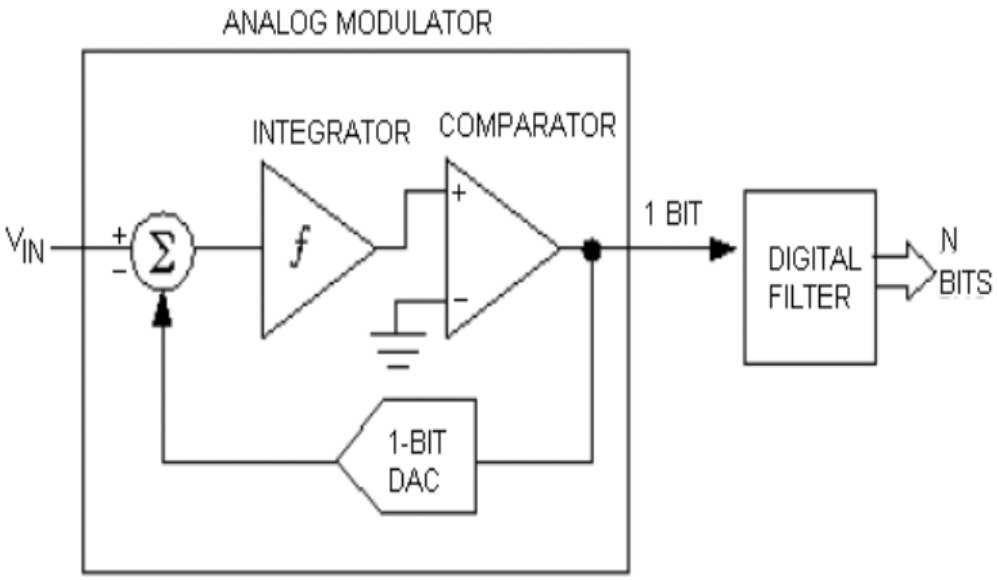


Figure 2.3: Block Diagram of Sigma Delta Converter [14]

The advantage of Sigma Delta ADC is its accuracy that is achieved by the input reference and clock rate. In the flash ADCs, the resistors affect the conversion accuracy that is not the case in sigma delta ADC. The other advantage of sigma-delta converter is its cost. The limitation of sigma-delta converter is its speed. It is the slowest architecture in all types of ADC architectures. This converter performs over sampling of the input for conversion. This conversion can takes places in many clock cycles. The other disadvantage of sigma-delta converter is the complexity in designing of the digital filter that is used to convert duty cycle information into digital word.

2.3.3 Pipelined ADC:

The pipelined analog-to-digital converter is one of the most popular ADC architecture. It can work from few Msamples to more than hundreds of Msamples with resolution from 8 bit to 16 bits. Due to its high resolution and sampling rate range it is widely use in medical and communication applications e.g. CCD imaging, digital receiver, digital video, xDSL, cable modem, and fast Ethernet. Speed, resolution, power and dynamic performance are greatly improved in Pipeline ADC but SAR and integrating architectures are still used for low sampling rate applications, whereas for high sampling rate (e.g. 1 Ghz) flash ADC is still the choice. The example of 12 bits pipeline ADC is shown in figure 2.4.

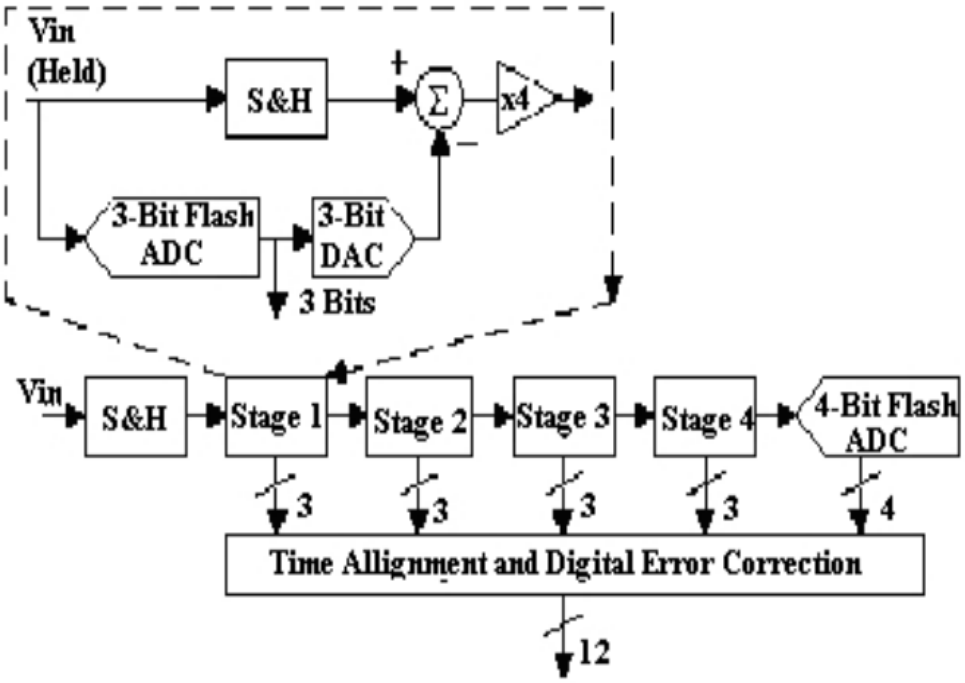


Figure 2.4: Pipelined ADC with four 3-bit stages (each stage resolves 2 bits) [14]

Initially sample-and-hold (S&H) circuit, samples and holds the input V_{IN}. The flash ADC in the first stage will convert this signal into 3 bit digital output. This 3 bits digital code is applied to DAC and the analog output is subtracted from the original signal, then the remainder is multiplied by 4 and then applied to the next stage. This process will continue till the last stage (stage 4) and every stage provides 3 bits. At last stage the amplified remainder signal is feed into 4 Bit flash ADC that will generate 4 least significant bits. As every stage generates bits at different instant in time therefore it is required to align all the bits by shift register prior to applying 12-bit digital output to the digital-error-correction logic. During the interval when one stage completes the processing of one sample and passes the magnified remainder to the other stage. The next stages are also performing the same operation because sample and hold circuit is embedded in every stage. This pipelining technique explained above increases the throughput of ADC.

2.3.4 Successive Approximation ADC:

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are mostly use in medium to high-resolution and low sampling rate applications. These are mostly in the range between 8 to 16 bits. It also provides small form factor and low power consumption. As its power

consumption is low therefore it is the good choice for low power application such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition. SAR ADC actually implements binary search algorithm, therefore its internal circuitry might work at several megahertz but due to the successive approximation algorithm the sampling rate of ADC is quite small. There are many ways to implement SAR ADC but its basic structure is shown in figure 2.5.

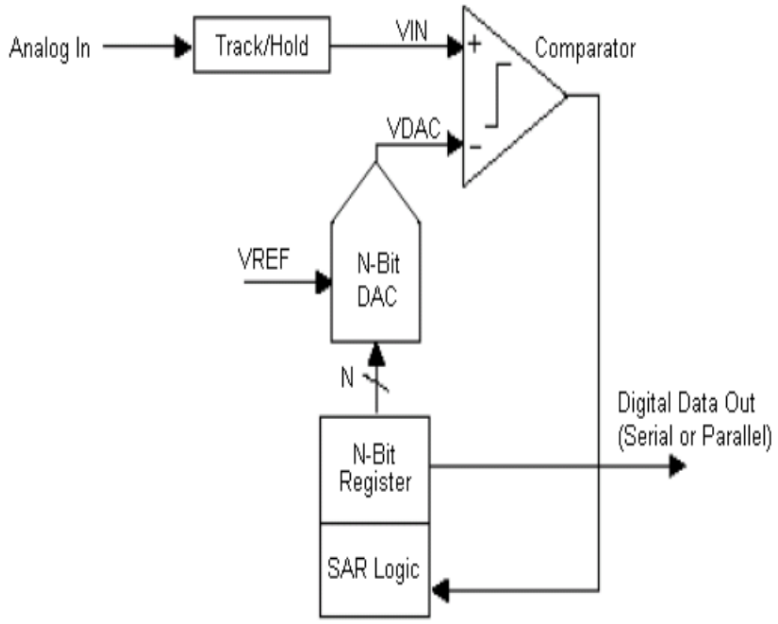


Figure 2.5: Simplified N-bit SAR ADC architecture [14]

In this structure track/hold circuit is used to hold the analog input voltage (V_{IN}). The binary search algorithm is implemented by N-bits register. Initially the value of register is set to mid-scale i.e. MSB set to "1" and all the other bits are set to "0". The output of DAC (V_{DAC}) becomes half the reference voltage $V_{REF}/2$, where V_{REF} is the reference voltage of ADC. The comparator will compare the input voltage V_{IN} with V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output will be set to "1", and the MSB of the N-bit register remains at '1'. If the input voltage V_{IN} is less than V_{DAC} then the comparator output becomes "0". The SAR control logic will change the MSB of the register to '0', set the next bit to "1" and perform comparison again. This process continues till LSB and once this process is completed the N-bit digital word is available in the register.

2.3.5 Dual-Slope ADC:

In order to understand the architecture of Dual slope ADC we first need to understand the concept of single slope ADC. The single slope ADC is also known as integrating ADC and the main theme of this architecture is to use analog ramping circuit and digital counter instead of using DAC. The op-amp circuit that is also called an integrator is used to generate a reference ramp signal that will compare with input signal by a comparator. The digital counter clocked with precise frequency is used to measure time taken by the reference signal to exceed the input signal voltage. The Dual-Slope ADC input voltage (V_{IN}) integrates for fixed time interval (T_{INT}), then it will de-integrate by using reference voltage (REFV) for a variable amount of time ($T_{DE\text{-}INT}$) as shown in Figure 2.6.

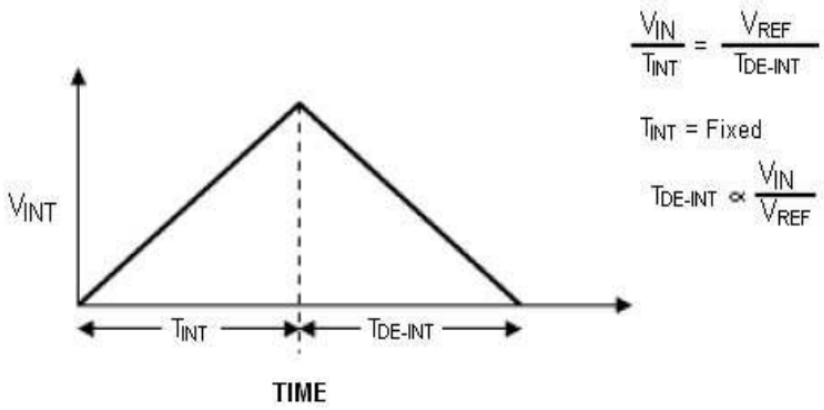


Figure 2.6: Dual-slope integration [14]

The behaviour of this structure is similar to digital ramp ADC, except that saw-tooth waveform is used as reference. “Integrating ADCs provides high resolution and can provide good noise rejection and line frequency”. As dual slope structure integrates input signal for fixed time instant therefore input signal becomes average and this will produce output with greater noise immunity. Due to this fact it is very useful for high accuracy applications. The other advantage of this structure is that it avoids DAC in the structure that decreases the design complexity. The main limitation of this structure is that it only suitable for low bandwidth input signals.

2.4 ADC comparison:

Table 2.1 shows the range of resolutions, conversion method, encoding method, conversion time, size, advantages and disadvantages available for flash, sigma-delta, successive approximation, pipeline, dual slope converters. As one can observe that flash ADC provide the

highest speed amongst all the other types of ADC. The speed of sigma delta converter is comparable with SAR ADC but even it is much slower than flash ADC. From the resolution point of view successive approximation resolution that is from 8 to 16 bits is comparable with pipelined structure but the fastest flash has maximum resolution of 6 to 8 bits. Therefore we can conclude that it is always the trade-off between speed, accuracy and power. The selection of architecture is mainly dependent upon the application.

Table 2.1: Comparison of ADC Architectures [30]

	FLASH (Parallel)	**SAR**	**PIPELINE**	**SIGMA DELTA**
Pick This Architecture if you want:	Ultra-High Speed when power consumption not primary concern?	Medium to high resolution (8 to 16bit), 5Msps and under, low power, small size.	High speeds, few Msps to 100+ Msps, 8 bits to 16 bits, lower power consumption than flash.	High resolution, low to medium speed, no precision external components
Conversion Method	N bits (2^N -1) comparators Caps increase by a factor of 2 for each bit.	Binary search algorithm, internal circuitry runs higher speed	Small parallel structure, each stage works on one to a few bits.	Oversampling ADC, 5-Hz- 60Hz rejection programmable data output
Encoding Method	Thermometer Code Encoding	Successive Approximation	Digital Correction Logic	Over-Sampling Modulator, Digital Decimation Filter
Disadvantages	Sparkle codes / metastability, high power consumption, large size, expensive	Speed limited to ~5Msps. May require anti-aliasing Filter	Parallelism increases throughput at the expense of power and latency	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC

Conversion Time	Conversion Time does not change with increased resolution.	Increases linearly with increased resolution.	Increases linearly with increased resolution	Tradeoff between data output rate and noise free resolution
Resolution	Component matching typically limits resolution to 8 bits.	Component matching requirements double with every bit increase in resolution.	Component matching requirements double with every bit increase in resolution	Component matching requirements double with every bit increase in resolution.
Size	2^N -1 comparators, Die size and power increases exponentially with resolution.	Die increases linearly with increase in resolution	Die increases linearly with increase in resolution	Core die size will not materially change with increase in resolution.

All families of converters are speed up with the CMOS process improvements e.g. successive approximation conversion time has been increased to tens of microseconds. This also effects the power consumption of data converters. On the other hand improvement in DSP functionality also impacts on the ADC design e.g. improvement in sigma-delta converter by adding fast and more complex digital filter.

CHAPTER 3

ADC CHARACTERIZATION

3.1 Basic ADC concepts and terminology:

Fundamentally analog to digital conversion involves sampling the analog signal and processing the sampled signal to generate the digital output bits. The rate at which the input signal is converted to its digital form determines the conversion speed and the number of output bits represents the resolution of the ADC. Some of the basic concepts of ADC are explained below.

1 Input Signal Bandwidth:

The frequency range of the input signal which can pass through the analog front end circuitry with minimal amplitude loss is called the bandwidth of input signal. For a sinusoidal signal, it is referred to as the frequency at which the amplitude is reduced by 70.7 % of original amplitude.

2 Resolution:

The smallest amplitude change in the input signal that can be distinguished by an ADC is called resolution. This can be calculated in terms of full scale voltage of input, but is typically represented as the number of bits used to represent the output digital signal. As High the number of output bits better is the resolution. For instance, a 4 bit ADC divides the input signal into sixteen levels while a 6 bit ADC divides the signal into sixty four steps consequently giving better resolution. The size of each step which is equal to LSB bit voltage is given by FSR/2N where FSR is the full scale range of the input.

3 Sample Rate:

The first step towards conversion of analog to digital is sampling. Sample rate or sampling frequency is defined as the number of samples of the input signal taken per second. According to the Nyquist theorem, for any band limited signal with maximum frequency Fmax, the sampling frequency (Fmax) must be at least equal to or greater than twice Fmax in order to reconstruct the signal properly. This implies that if the sampling frequency is less than twice Fmax, the signal cannot be reconstructed perfectly and higher the number of samples better would be its reconstruction. This concept is depicted in figure 3.1.

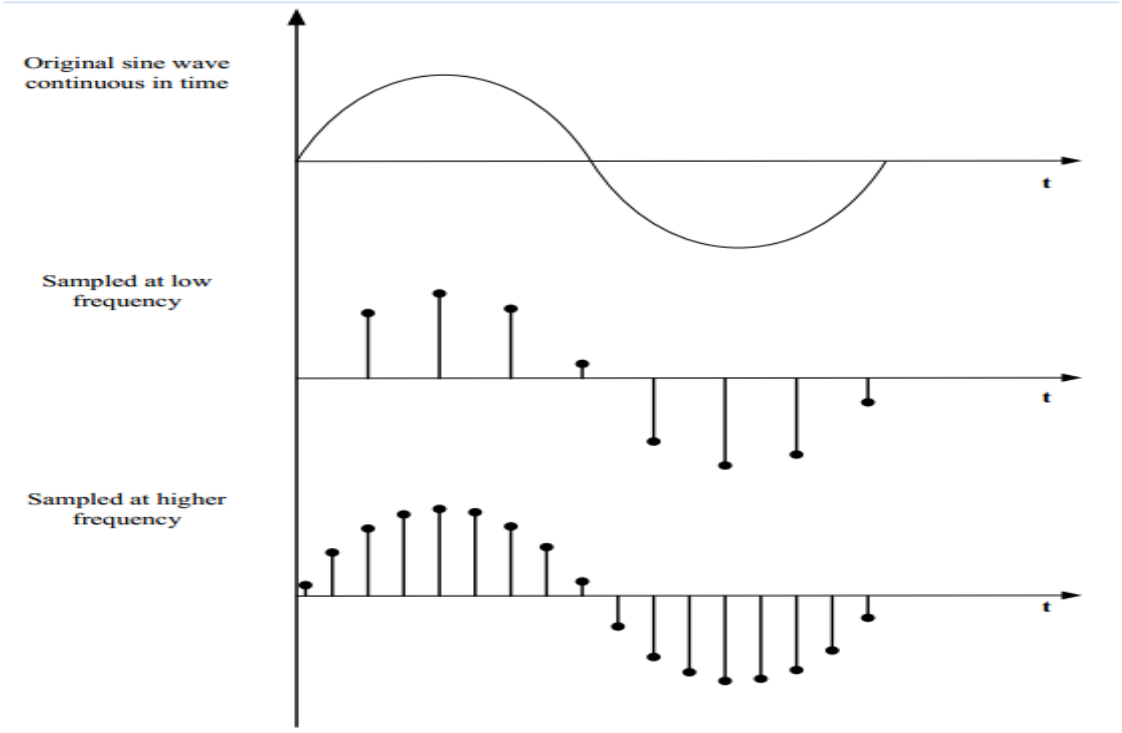


Figure 3.1 Sampled signal representation of a sinusoidal signal [

4 Signal to Noise Ratio (SNR):

By definition, SNR is the ratio of full scale value to the rms value of the quantization noise. The rms value is the root mean square value of quantization noise. It is the measure of signal power relative to the noise power.

$$SNR = 10 \log(\frac{Psignal}{Pnoise}) \quad 3.1$$

5 Effective Number of Bits (ENOB):

ENOB is a measure of actual performance of an ADC, which gives the conversion bit of an ADC. ENOB is calculated as shown below

$$ENOB = \frac{SNR-1.76}{6.02} \quad 3.2$$

6 Quantization Error:

While converting the analog signal to digital or in other words digitizing the analog signal, with a finite resolution ADCs there exists a certain amount of uncertainty termed as quantization error or quantization noise.

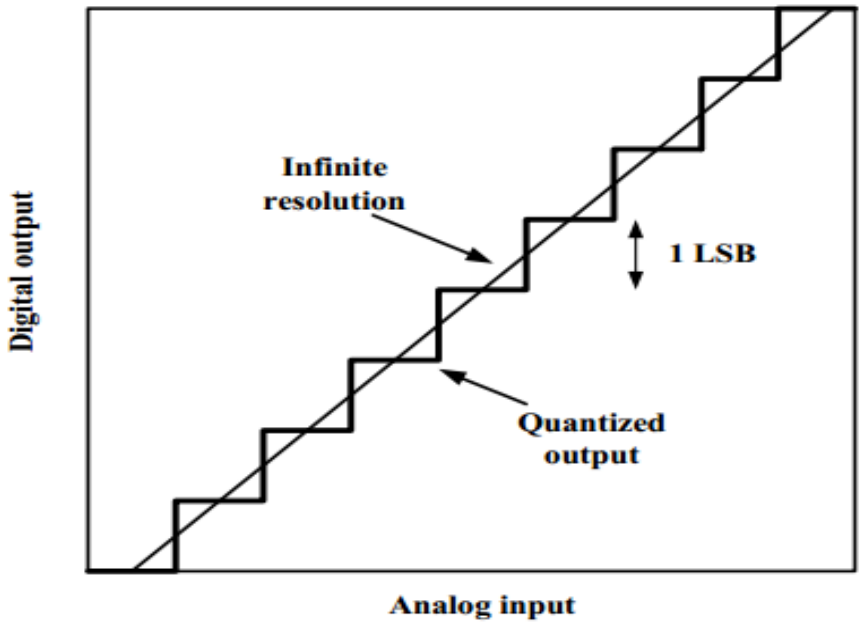


Figure 3.2 Ideal input -output characteristics of an ADC

The ideal input - output characteristics of an ADC are shown in figure 3.2.It is the difference between actual analog signal value and its quantized digital value.

7 Spur- Free Dynamic Range (SFDR):

SFDR is the ratio of the strength of the fundamental frequency to the strongest spurious signal in the output of ADCs. SFDR is an indicator of fidelity of an ADC. Non-linearity in the ADC generates spurious signals that affect the achievable SFDR.SFDR can be calculated using the below formula

$$\text{SFDR}=\text{Signal (dB)} - \text{largest spur (dB)} \qquad 3.3$$

8 Differential non- linearity (DNL):

DNL is a measure of separation between adjacent levels measured at vertical jump. DN L measures any deviation from one LSB. In other words, for an ideal ADC, the output is divided into 2^N uniform voltage levels, each with width. Any deviation from the ideal step width is called differential non- linearity (DNL) and is measured in number of counts (LSBs). The DNL is 0LSB for ideal ADCs. In a practical ADC, DNL error comes from its architecture. For example, in a SAR ADC, DNL error may be caused near the mid-range due to mismatching of its DAC.

Let us consider an example of a 3-bit ADC with transfer characteristics as shown in Figure 3.3. In this ADC, each input step should be exactly 1/8 of the full-scale input range (1 LSB of this ADC). Given that this ADC has an input range from 0V to 8V, the first output-code transition is caused by an input change of 0.5V (Full-scale input range/16 = 0.5 LSB), which is as expected.

However, the second transition, from 001 to 010, takes place after an input change of 1.25V (1.25 LSB), and so is too large by 0.25 LSB. Similarly, there is a variation in step size at each of the following steps. The DNL of this particular ADC can be specified as 0.75 LSB, which is the maximum deviation from the ideal step size of this ADC throughout its transfer.

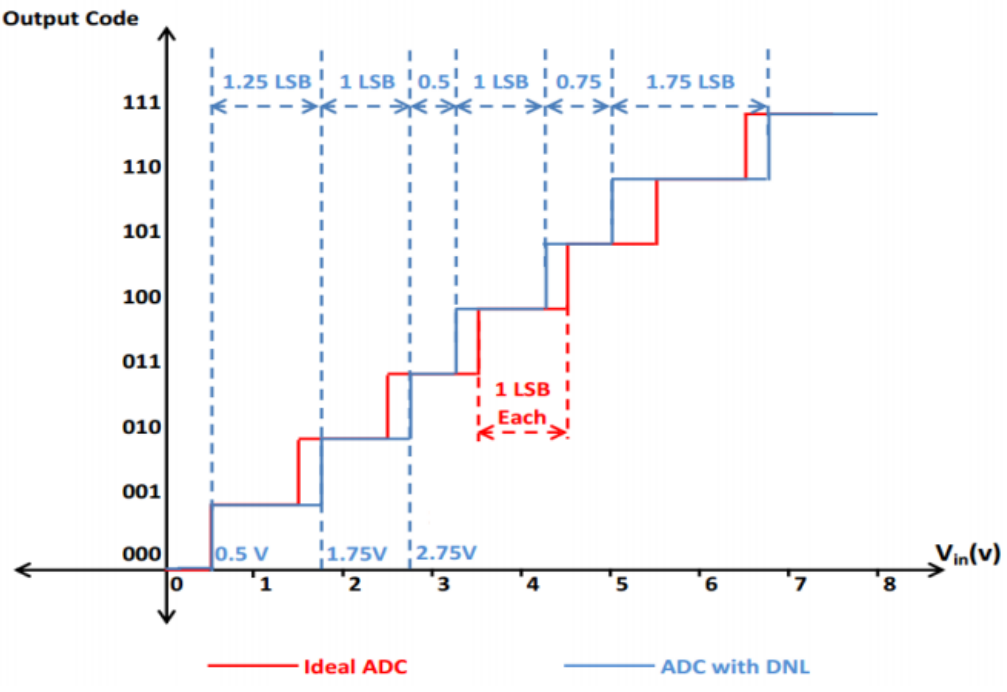


Figure 3.3 Representation of DNL in an ADC transfer curve

9 Integral non-linearity (INL):

Integral non linearity (INL) is the maximum difference between actual finite resolution characteristic and ideal finite resolution characteristics. In the other words INL is a measure of how closely the ADC output matches its ideal response. INL can be defined as the deviation in LSB of the actual transfer function of the ADC from the ideal transfer curve. INL can be estimated using DNL at each step by calculating the cumulative sum of DNL errors up to that point. In reality, INL is measured by plotting the ADC transfer characteristics as explained below.

There are two methods to find the INL error

1. Best fit (best straight line) method
2. End point method

Best fit (best straight line) method:

The best fit method of INL measurement considers offset and gain error. One can see in Figure 3.4 that the Ideal transfer curve considered for calculating best-fit INL does not go through the origin. The ideal transfer curve here is drawn such that it depicts the nearest first-order approximation to the actual transfer curve of the ADC. The intercept and slope of this ideal curve can lend us the values of the offset and gain error of the ADC. Quite intuitively, the best fit method yields better results for INL.

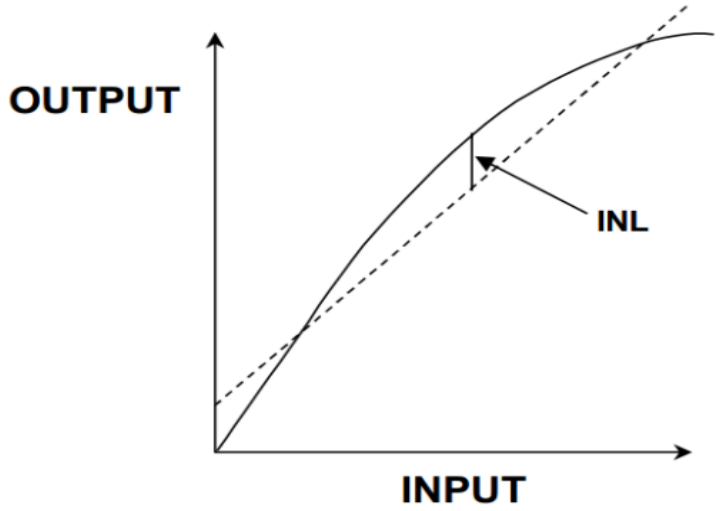


Figure 3.4 Best Fit INL

The only real use of the best fit INL number is to predict distortion in AC applications. This number would be equivalent to the maximum deviation for an AC application

End-point INL:

The End-Point method provides the worst case INL. This measurement passes the straight line through the origin and maximum output code of the ADC. (Refer Figure 3.5). As this method provides the worst case INL, it is more useful to use this number as compared to the one measured using best fit for DC applications. The parameter INL must be considered for applications involving precision measurements and control.

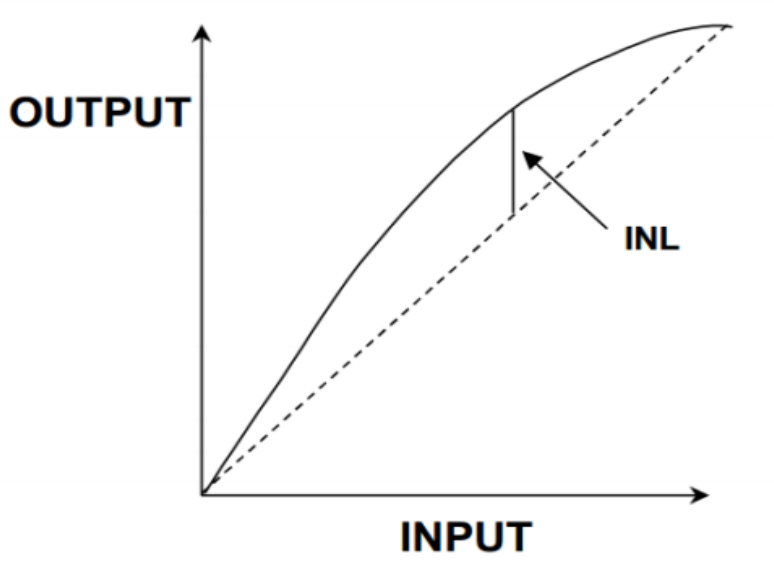


Figure 3.5 Endpoint INL

CHAPTER 4

FLASH A/D CONVERTER

Introduction

CMOS Logic Design

Components of Flash ADC

4.1 Introduction:

As we have seen in the previous chapter that the best- known architecture for a high speed Analog-to-Digital converters is the Flash converter structure. The aim of our project is to design a high speed ADC with less power consumption in this chapter we will present you the Logic which is suitable for low power dissipation, basic component of the Flash ADC and give some basic understanding of each component.

4.2 CMOS Logic Design:

In Flash ADC design the most important thing is to decide the CMOS logic design. There are various types of CMOS logic design

4.2.1 Static CMOS Design:

Static CMOS is a design methodology only in combinatorial logic circuits. A static logic gate is one that has a well-defined output once the inputs are stabilized and the switching transients have decayed away. Static CMOS logic gates are relatively easy to design and use. A static CMOS gate is a combination of pull-up network and pull-down network as shown in figure 4.1.

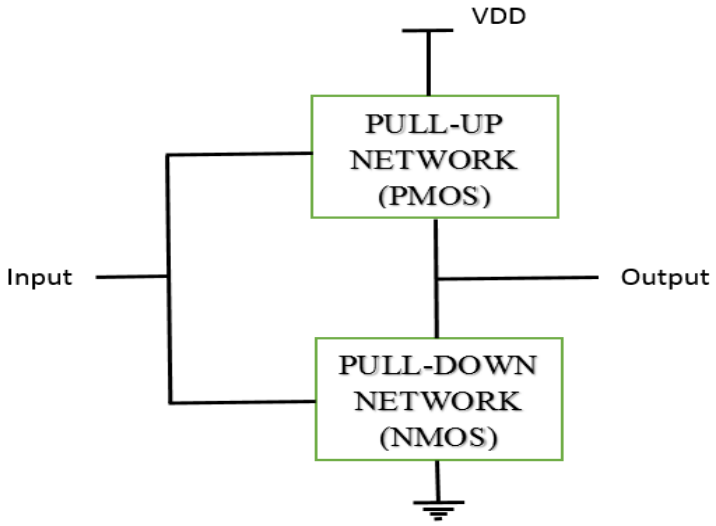


Figure 4.1 Static Logic style

The function of the PUN is to provide a connection between the output and V_{DD} anytime the output of the logic gate is meant to be 1(based on inputs). Similarly the function of the PDN is to provide a connection between the output and GND anytime the output of the logic gate is meant to be 0(based on inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one network is conducting in steady state. In this way, once the transient have settled, a path always exits between V_{DD} and the output or GND and the output.

4.2.2 Dynamic CMOS Design:

Dynamic logic (or sometimes clocked logic) is a design methodology in combinational logic circuits, particularly those latch which is implemented in MOS technology. Dynamic logic uses a clock signal in its implementation of combinational logic circuits. The use of a clock signal is to synchronize transitions in sequential logic circuits. The dynamic CMOS logic style is shown in figure 4.2. For most implementations of combinational logic, a clock signal is not even needed.
Operation of the circuit is divided into two phases:

1. Precharge Phase
2. Evaluation Phase

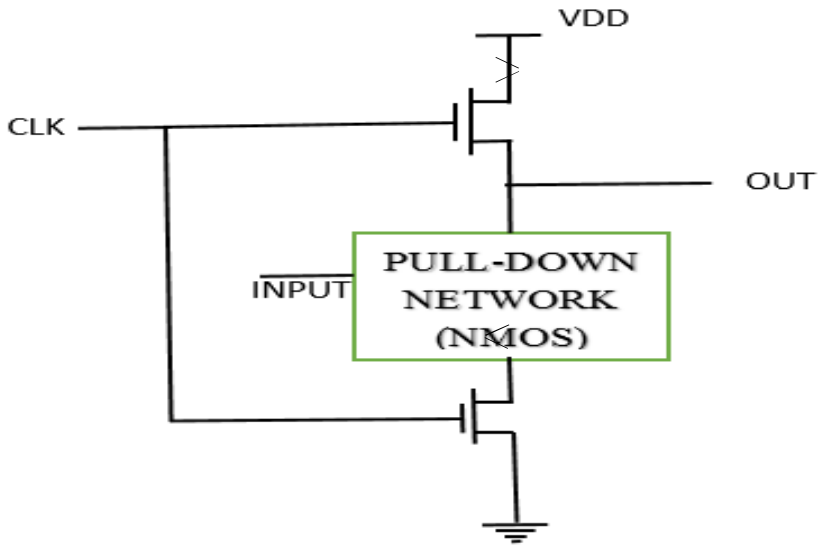


Figure 4.2 Dynamic Logic style

In the precharging phase (CLK = 0) output node is precharged to VDD by the pullup PMOS transistor. The pull down network is off during this time independent of the condition of the other NMOS transistors, since one of the NMOS transistor id off which is connected to clock. This eliminates any static power which will be consumed during the precharging period. In the Evalution phase CLK =1, the precharge transistor (PMOS transistor in the pull up path) is off and one of the NMOS transistor which is connected to CLK is switched on. The output is evaluated during this time depending upon the NMOS transistor conditions in the pull down network.

Dynamic logic implementation has faster switching speed in comparison with static CMOS because of the lower number of transistors required for implementation and single transistor load per fan in. Dynamic CMOS logic circuits are usually faster than static CMOS logic circuit, and require less chip area, but are more difficult to design, and have higher power dissipation. In order to avoid static power dissipation and to achieve moderate speed, the implementation is done using dynamic CMOS logic.

4.3 Components of Flash ADC:

In flash ADC an array of comparators compares the input voltage with a set of increasing reference voltages. The comparator output represents the input signal in a thermometer code, which will then convert into binary code. By this description we can easily understand that almost all flash ADC comprises of following three blocks:

1. Resistor Ladder Block
2. Comparator Block
3. Decoder Block

In the next sections we will give the description of each block.

4.3.1 Resistor Ladder:

In a flash Analog-to-Digital Converter, resistor ladder block is used to generate the reference voltages for the comparators. The block diagram of resistor ladder is shown in figure 4.3.

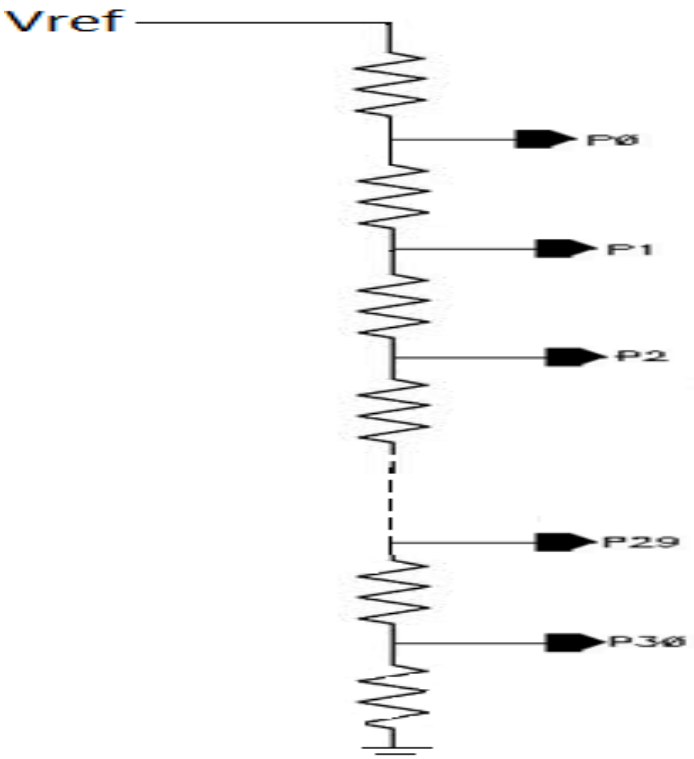


Figure 4.3 Resistor Ladder Block

There are two various option to put the resistor

1. Using simple Resistor
2. Using resm9 Resistor
3. Using NMOS as Resistor

4.3.1.1 Using simple Resistor:

In this we use the simple analog resistor but the problem with analog resistor is bulky, cover more area, noisy etc. so the simple analog resistor is not a better choice for making resistor ladder

4.3.1.2 Using resm9 Resistor:

In this we use the resm9 from the gpdk90nm library of the cadence tool. The advantage of using resm9 resistor is less area covered with respect to the analog resistor, less noisy etc.

4.3.1.3 Using NMOS as a Resistor:

In this we use NMOS as a resistor. It is the best choice for resistor ladder because the NMOS resistor require less area as compared to any type of resistor but NMOS resistor behave as a non-linear resistor. So the design challenge of NMOS resistor, NMOS is work in the linear region. The NMOS used as a resistor is shown in figure 4.4.

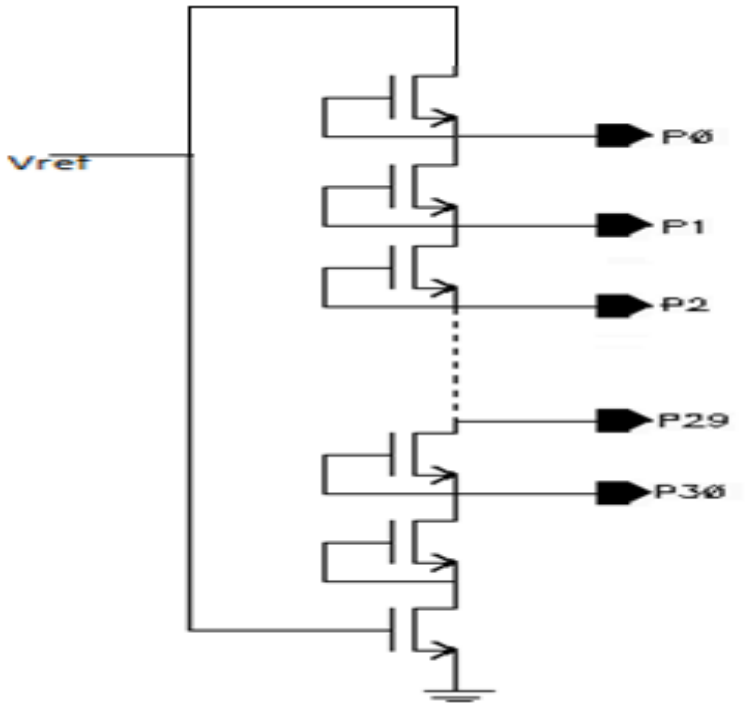
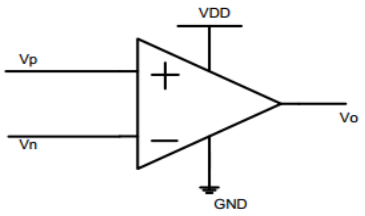


Figure 4.4 Resistor Ladder Block using NMOS as a resistor

4.3.2 Comparator Block:

A comparator is used to detect whether a signal is greater or smaller than reference signal. Comparators are widely used in A/D converter design.



$V_P < V_N$ then V_O = VSS= logic 0.

$V_P > V_N$ then V_O = VDD= logic 1.

Figure 4.5 Comparator operation

The diagram of comparator is shown in figure 4.5. If the +, V_P, the input of the comparator is at a greater potential than the -, V_N, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the –input, the output of the comparator is at logic 0.

The block diagram of comparator block is shown in figure 4.6.

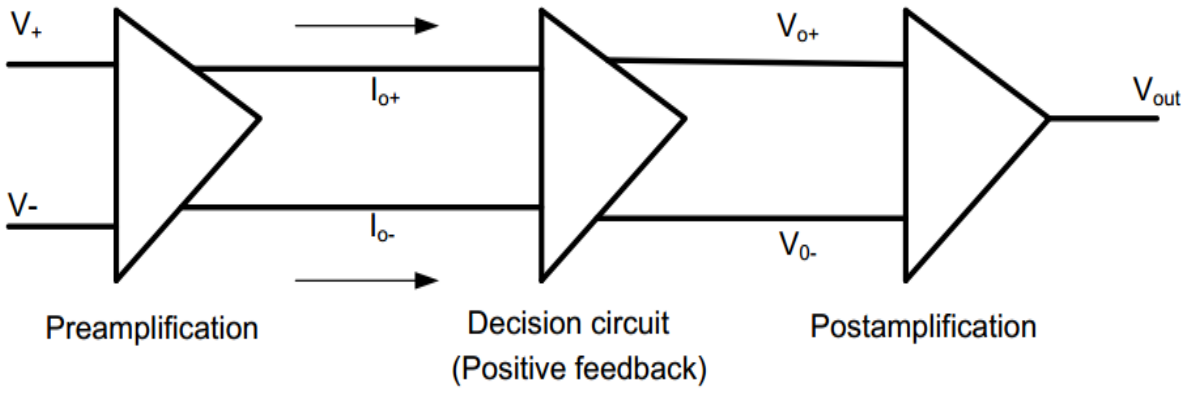


Figure 4.6 Block Diagram of Comparator

It is also found in many other applications such as data transmission, switching power regulators and others. There are so many techniques to design a comparator such as multiple stage comparators, positive feedback, track and latch comparators, and fully differential comparators. Low power consumption is an important feature of many A/D converters especially those used in portable devices that have limited power supply energy. A common technique to reduce its power is the adoption of a latch comparator design. Dynamic latch comparator can solve the power problem by removing the pre-amplifying stage, while achieving a less area. Although latched comparators typically have a high offset voltage in the range of 100mV, their fast speed and low power make them suitable for several applications. In this project we are using “Latched Comparator”.

In this we use three stage CMOS latched Comparator in which there are three stages of latched comparator are:

1. Preamplifier
2. Latch
3. Output Buffer

4.3.2.1 Preamplifier:

The pre-amplifier at the comparator inputs consists of a differential amplifier with resistances as load. The pre-amplifier is used to reduce the input offset and kickback noise. The pre-amplifier circuit is shown in figure 4.7.

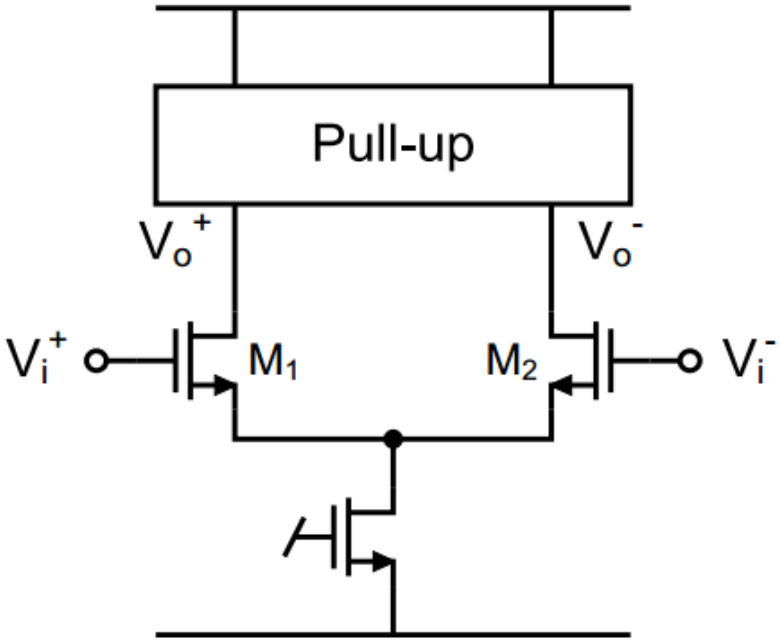


Figure 4.7 Circuit of Pre-amplifier [2]

The pre-amplifier amplifies the difference between input voltage and the reference voltage generated by the resistive ladder of the ADC. The pre-amplifier is a circuit which is used to amplify the signal so that it can easily drive the load. In most latched comparator design of pre-amplifiers are also used to avoid the kickback effect from the latch and input referred offset.

Gain accuracy is the worst for resistive pull-up as resistors (poly, diffusion, well, and etc.) don't track transistors. NMOS pull-up suffers from body effect, affecting gain setting accuracy.

4.3.2.2 Latch:

Basic function of the latch in any circuit is as a memory element, which is used to store the value. Latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. There are various types of latch

1 Static Latch

2 Semi-Dynamic Latch

3 Dynamic Latch

Latches and flip-flips can be static or dynamic. A dynamic latch or flip-flop gradually loses its content as time goes, while a static one retains its content no matter how much time is elapsed. The charge will leak out of the output capacitor of the dynamic latch as time goes and thus the content of the latch is lost. So the use of a dynamic latch should be carefully scrutinized.

4.3.2.2.1 Static latch:

The static latch circuit is shown in figure 4.8. The operation of static latch is described in two part: first is Φ (clock signal) is 0 and second is Φ is 1. Active pull-up and pull-down →full CMOS logic levels is present in the static latch. Static latch is Very fast. The output Q+ and Q- are not well defined in reset mode (Φ= 1). In the static latch a large short-circuit current is in reset mode. Due to which the power dissipation is more. There is zero DC current after full regeneration.

The speed of the static latch is high but the average power dissipation is more so the static latch is not a good choice for low power Flash ADC.

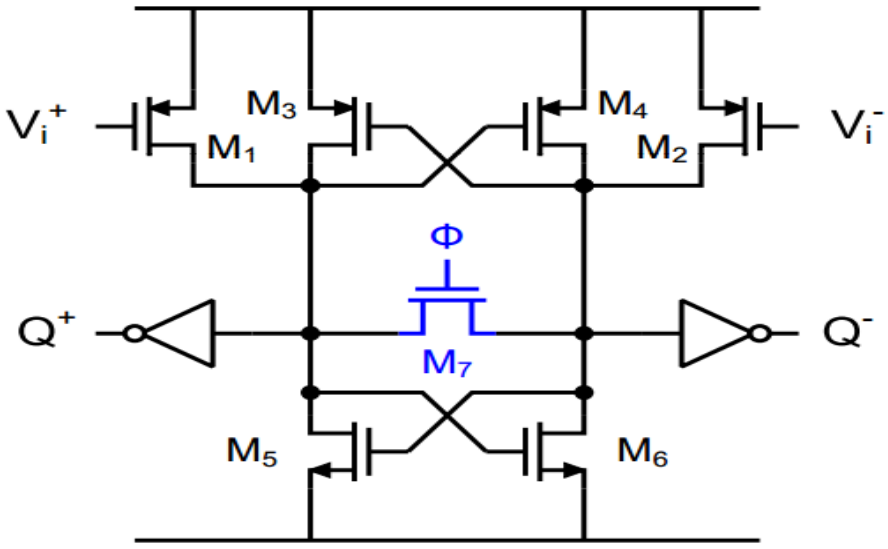


Figure 4.8 Circuit of Static Latch circuit [5]

4.3.2.2.2 Semi Dynamic Latch:

The static latch circuit is shown in figure 4.9. The operation of static latch is described in two part: first is Φ (clock signal) is 0 and second is Φ is 1. In the semi dynamic latch diode divider disabled in reset mode due to which less short-circuit current flow.

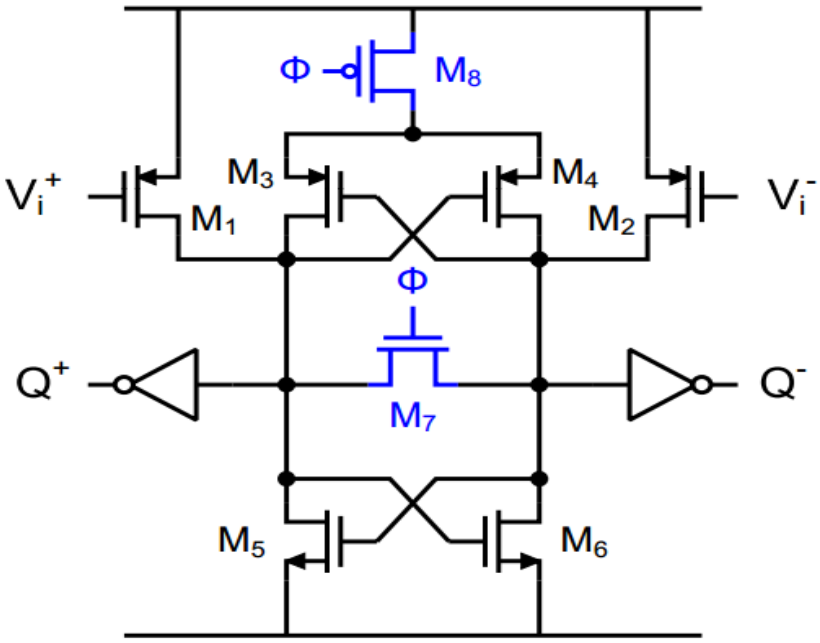


Figure 4.9 Circuit of Semi-Dynamic Latch circuit [5]

The Pull-up of semi dynamic latch is not as fast. The problem with semi-dynamic latch is that the output Q+ and Q- are still not well defined in reset mode (Φ= 1). There are zero DC current after full regeneration. The semi-dynamic latch are still very noisy.

4.3.2.2.3 Dynamic Latch:

A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. The circuit is driven by a clock. During one phase of the clock (clk =high) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk = low), the transmission gate opens and the inverter's output is determined by the node. The Setup and hold times determined by the transmission gate must be taken in consideration in order to ensure proper operation of the dynamic latch i.e.

adequate level of voltage is stored in the gate capacitance of the latch. A simple dynamic latch is shown in figure 4.10.

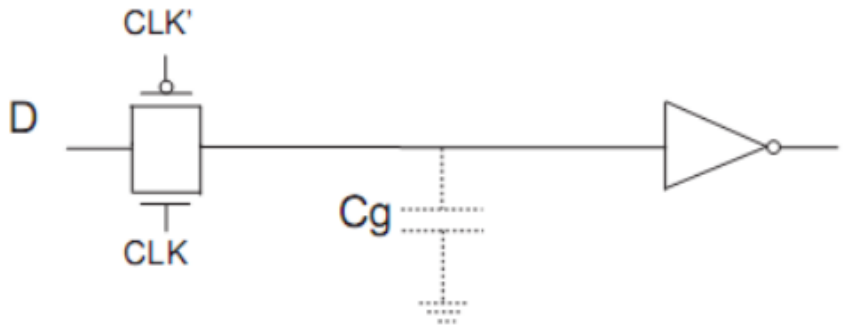


Figure 4.10 Simple dynamic latch.

The dynamic latch circuit is shown in Fig. 4.11. The operation of dynamic latch is described in two part: first is Φ (clock signal) is 0 and second is Φ is 1.

When Φ = 0: M7, M8 is ON and M5, M6 gate node is connected to the high voltage so both PMOS is in OFF state. The NMOS M9, M10 is in OFF state so there is no change in output.

When Φ = 1: The NMOS M9, M10 is ON and PMOS M7, M8 is OFF so let Q^+ is high then the gate of M6 is high and M6 is ON

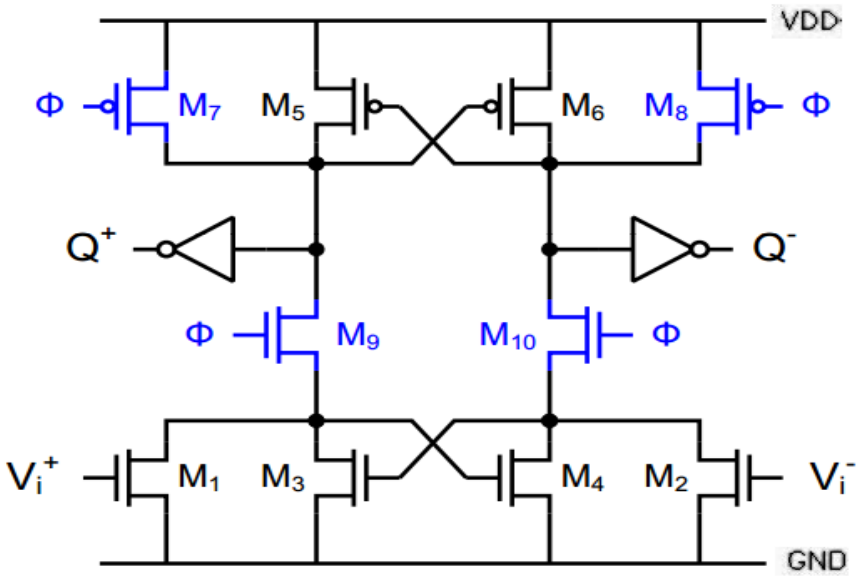


Figure 4.11 Circuit of Dynamic latch [17]

4.3.2.3 Output Buffer:

The final component in our comparator design is the output buffer or post-amplifier. The aim purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V). The schematic of output buffer is shown in figure 4.12.

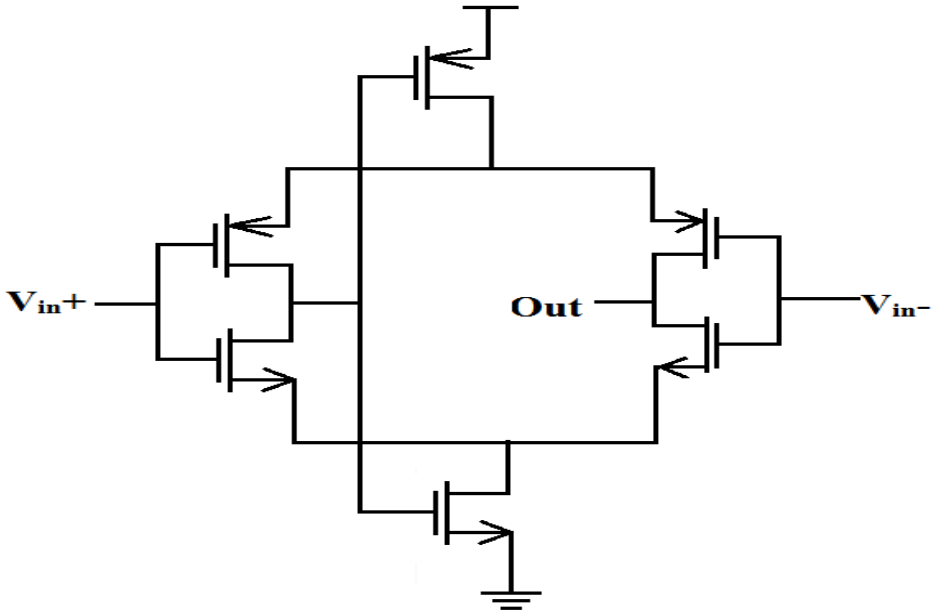


Figure 4.12 Circuit of Output Buffer

The ideal transfer characteristic of comparator is shown in figure 4.13.

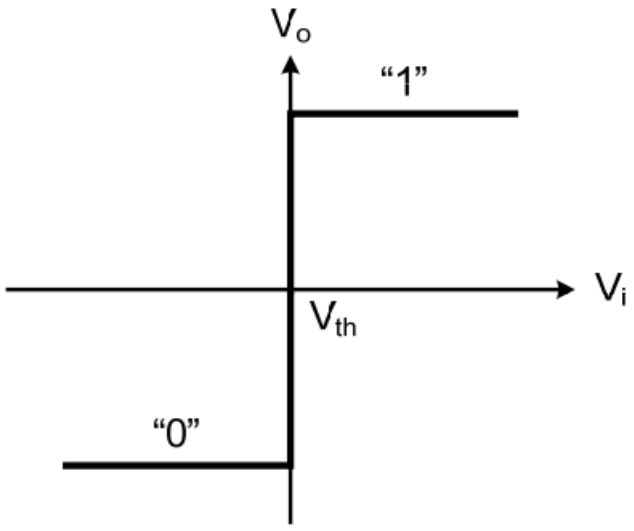


Figure 4.13 Transfer characteristic of comparator (ideal)

4.3.3 Encoder Block:

Designing of converting thermometer code into binary code is one of the main design issues of any flash ADC encoder [4]. There are various methods of converting thermo-meter-code to binary code

1. **Thermo-meter-code- to other than other to binary code:**

In this conversion there are one intermediate stage due to this the extra intermediate stage the parameters like power dissipation, current dissipation, propagation delay etc. are increases.

2. **Direct conversion of thermo-meter-code to binary code:**

In this method, by the help of the truth table we made the equations of direct conversion of thermo-meter code to binary code. The advantage of this method is, the parameters like power dissipation, current dissipation, propagation delay etc. are decreases.

The truth table of thermometer code to binary code is shown in table 4.1:

Table 4.1 Truth table of Thermo-meter code to Binary code

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Thermometer code
0	0	0	0	0	0000 0000 0000 0000 0000 0000 0000 000
0	0	0	0	1	0000 0000 0000 0000 0000 0000 0000 001
0	0	0	1	0	0000 0000 0000 0000 0000 0000 0000 011
0	0	0	1	1	0000 0000 0000 0000 0000 0000 0000 111
0	0	1	0	0	0000 0000 0000 0000 0000 0000 0001 111
0	0	1	0	1	0000 0000 0000 0000 0000 0000 0011 111
0	0	1	1	0	0000 0000 0000 0000 0000 0000 0111 111
0	0	1	1	1	0000 0000 0000 0000 0000 0000 1111 111
0	1	0	0	0	0000 0000 0000 0000 0000 0001 1111 111

0	1	0	0	1	0000 0000 0000 0000 0000 0011 1111 111
0	1	0	1	0	0000 0000 0000 0000 0000 0111 1111 111
0	1	0	1	1	0000 0000 0000 0000 0000 1111 1111 111
0	1	1	0	0	0000 0000 0000 0000 0001 1111 1111 111
0	1	1	0	1	0000 0000 0000 0000 0011 1111 1111 111
0	1	1	1	0	0000 0000 0000 0000 0111 1111 1111 111
0	1	1	1	1	0000 0000 0000 0000 1111 1111 1111 111
1	0	0	0	0	0000 0000 0000 0001 1111 1111 1111 111
1	0	0	0	1	0000 0000 0000 0011 1111 1111 1111 111
1	0	0	1	0	0000 0000 0000 0111 1111 1111 1111 111
1	0	0	1	1	0000 0000 0000 1111 1111 1111 1111 111
1	0	1	0	0	0000 0000 0001 1111 1111 1111 1111 111
1	0	1	0	1	0000 0000 0001 1111 1111 1111 1111 111
1	0	1	1	0	0000 0000 0011 1111 1111 1111 1111 111
1	0	1	1	1	0000 0000 0111 1111 1111 1111 1111 111
1	1	0	0	0	0000 0000 1111 1111 1111 1111 1111 111
1	1	0	0	1	0000 0001 1111 1111 1111 1111 1111 111
1	1	0	1	0	0000 0011 1111 1111 1111 1111 1111 111
1	1	0	1	1	0000 0111 1111 1111 1111 1111 1111 111
1	1	1	0	0	0001 1111 1111 1111 1111 1111 1111 111
1	1	1	0	1	0011 1111 1111 1111 1111 1111 1111 111
1	1	1	1	0	0111 1111 1111 1111 1111 1111 1111 111
1	1	1	1	1	1111 1111 1111 1111 1111 1111 1111 111

The following equations gives the relation between the thermometer coded data and the binary coded data for a 5 bit encoder.

Bit 4 = I_{15}

Bit 3 = $I_7.\overline{I_{15}} + I_{23}$

Bit 2 = $I_3.\overline{I_7} + I_{11}.\overline{I_{15}} + I_{19}.\overline{I_{23}} + I_{27}$

Bit 1 = $I_1.\overline{I_3} + I_5.\overline{I_7} + I_9.\overline{I_{11}} + I_{13}.\overline{I_{15}} + I_{17}.\overline{I_{19}} + I_{21}.\overline{I_{23}} + I_{25}.\overline{I_{27}} + I_{29}$

Bit 0 = $I_0.\overline{I_1} + I_2.\overline{I_3} + I_4.\overline{I_5} + I_6.\overline{I_7} + I_8.\overline{I_9} + I_{10}.\overline{I_{11}} + I_{12}.\overline{I_{13}} + I_{14}.\overline{I_{15}} + I_{16}.\overline{I_{17}} + I_{18}.\overline{I_{19}} + I_{20}.\overline{I_{21}} +$

$I_{22}.\overline{I_{23}} + I_{24}.\overline{I_{25}} + I_{26}.\overline{I_{27}} + I_{28}.\overline{I_{29}} + I_{30}$

CHAPTER 5

FLASH ADC IMPLIMENTATION

RESISTOR LADDER BLOCK

COMPARATOR BLOCK

ENCODER BLOCK

Flash ADC Implementation

In this chapter we are giving the each block circuit. The implementation is done by using the dynamic CMOS logic style. The block of Flash ADC is divided into three major blocks:

5.1 Resistor Ladder Block:

Resistor ladder divide the reference voltage V_{ref} into 32 levels. Resistor ladder block is shown in figure 5.1. Here we use the 1KΩ resistor from analog library of the CADENCE Tool. In the Flash ADC we use the 32 resistor of value 1KΩ in series ladder as shown.

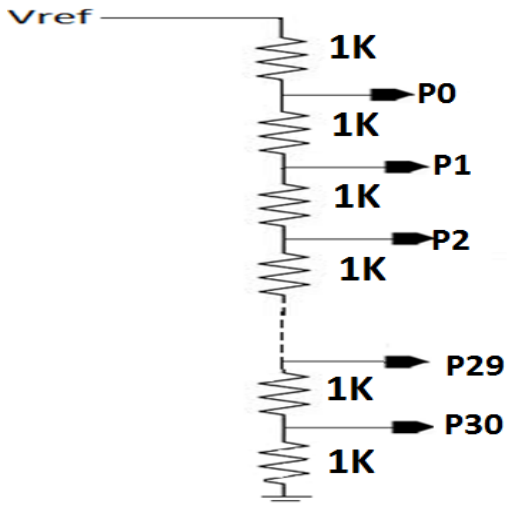


Figure 5.1 Resistor Ladder Block

The output of the resistor ladder is given to comparator block.

5.2 Comparator block:

5.2.1 Preamplifier Schematic and Layout

The pre-amplifier schematic and layout are shown in figure 5.2 and 5.3 respectively. The basic function of the pre-amplifier circuit is to amplify the difference of the input signals. By using the pre-amplifier the major advantage, it reduce the Kickback effect which is produced in the latch due to regenerative node. But the disadvantage, it increase the power dissipation of the comparator.

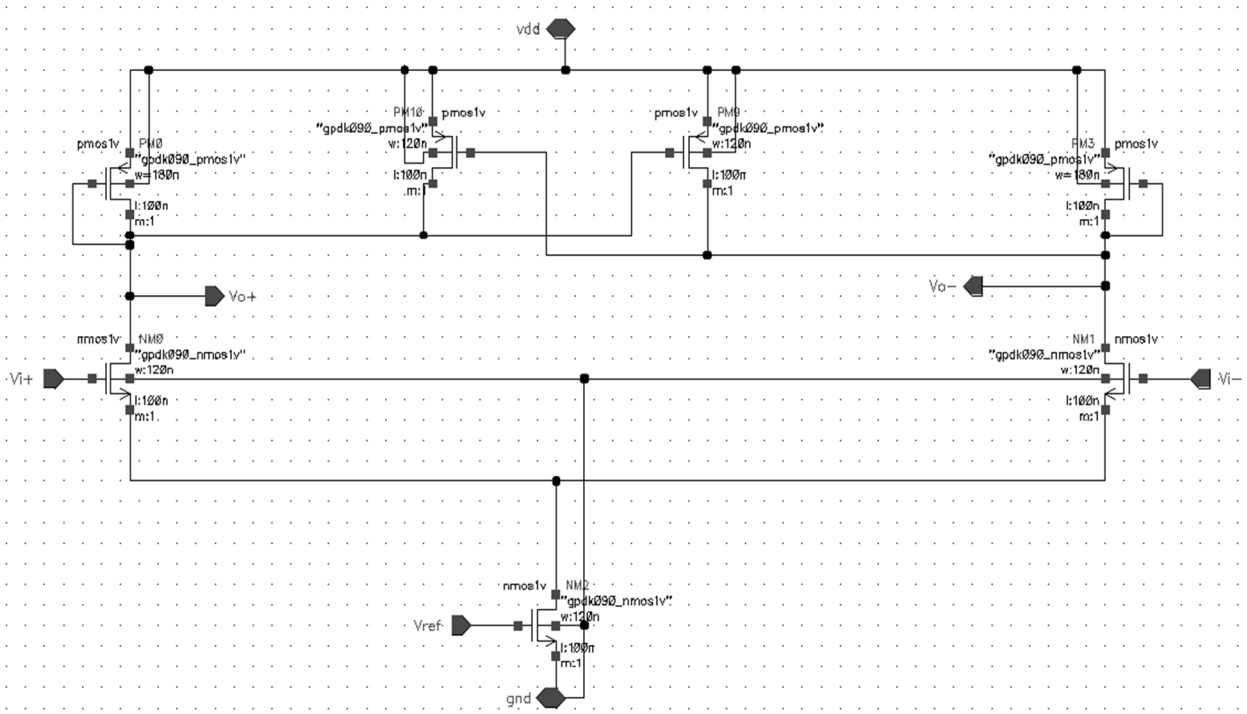


Figure 5.2 Preamplifier Schematic

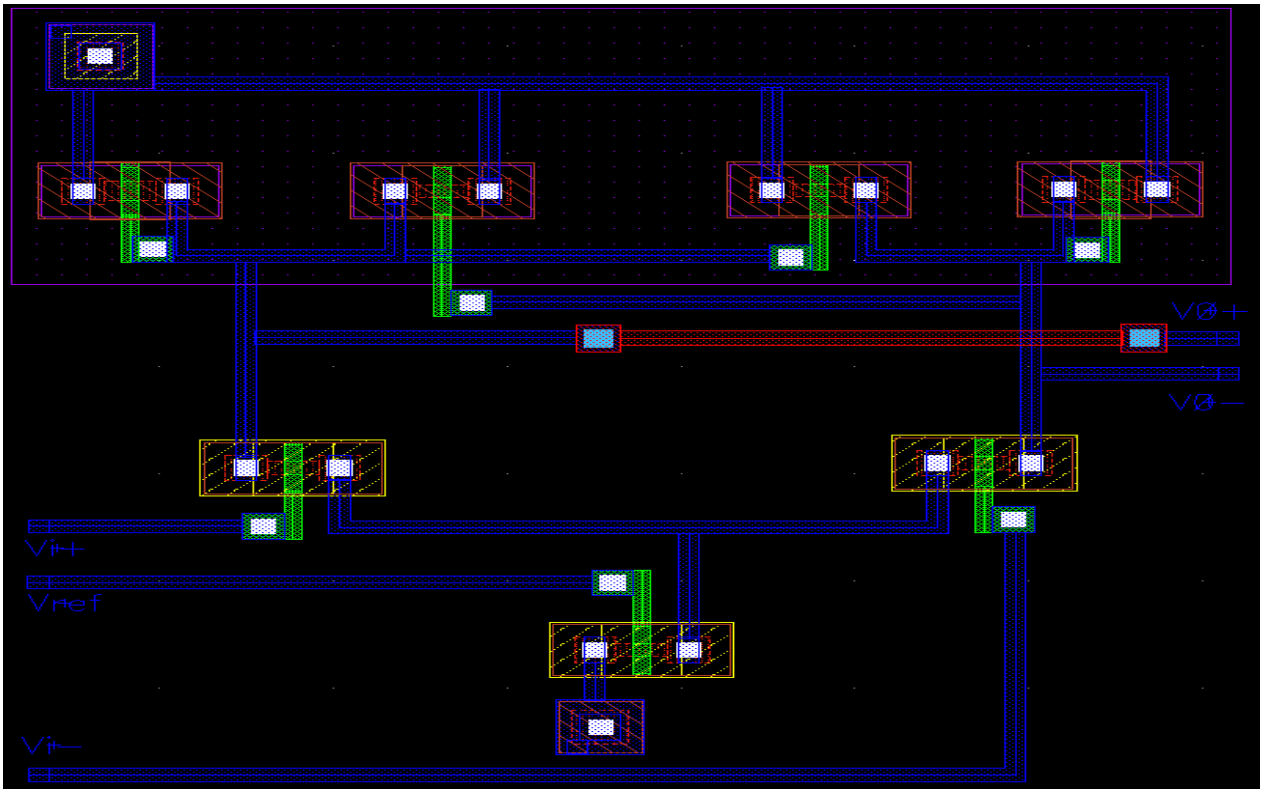


Figure 5.3 Preamplifier Layout

5.2.2 Dynamic Latch Schematic and Layout

The dynamic latch schematic and layout is shown in figure 5.4 and 5.5 respectively. The basic function is to sore the value of the output of pre-amplifier for the single clock cycle. The dynamic latch is slow but this circuit is synchronised by the clock signal

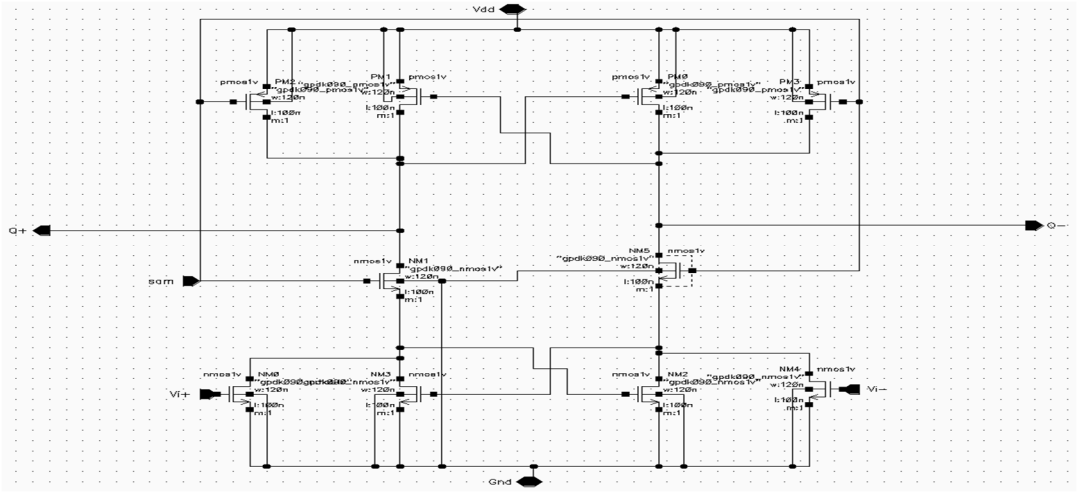


Figure 5.4 Dynamic Latch Schematic

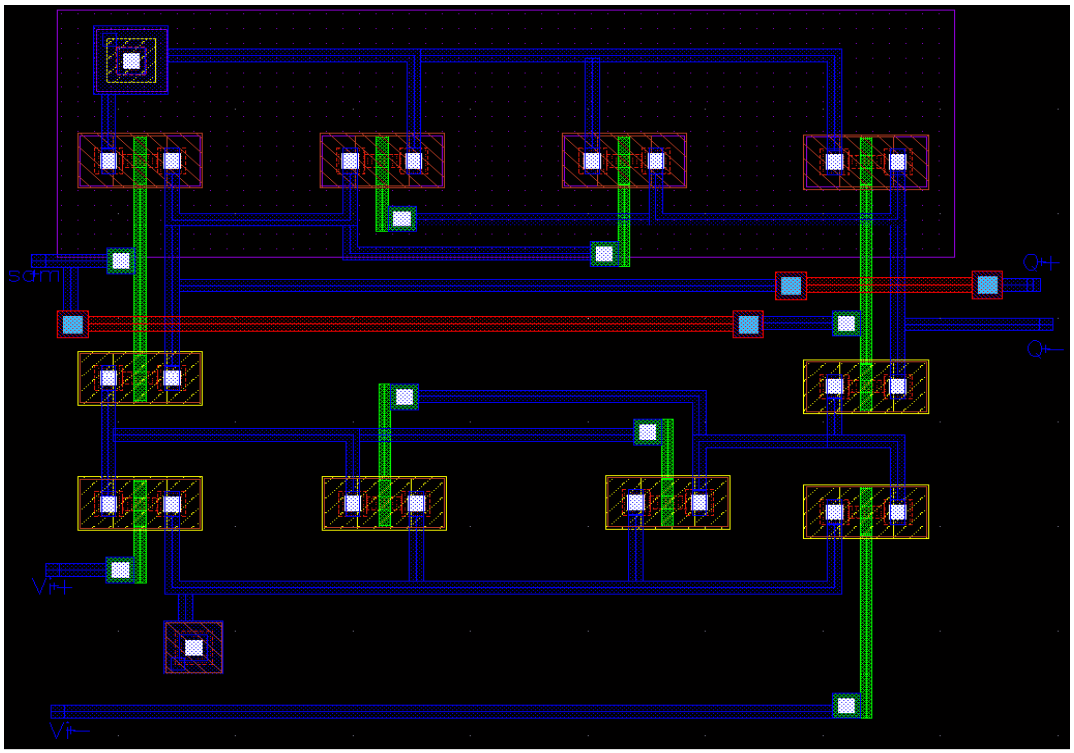


Figure 5.5 Dynamic Latch Layout

5.2.3 Output Buffer Schematic and Layout

The output buffer circuit and layout are shown in figure 5.6 and 5.7 respectively. The basic function is to take a differential input and give the single output.

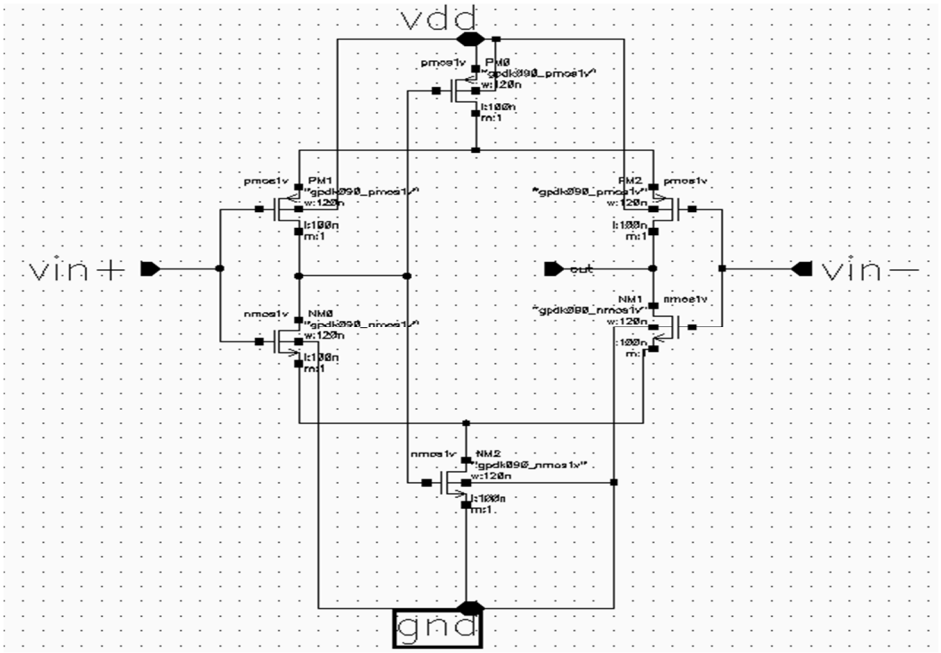


Figure 5.6 Output Buffer Schematic

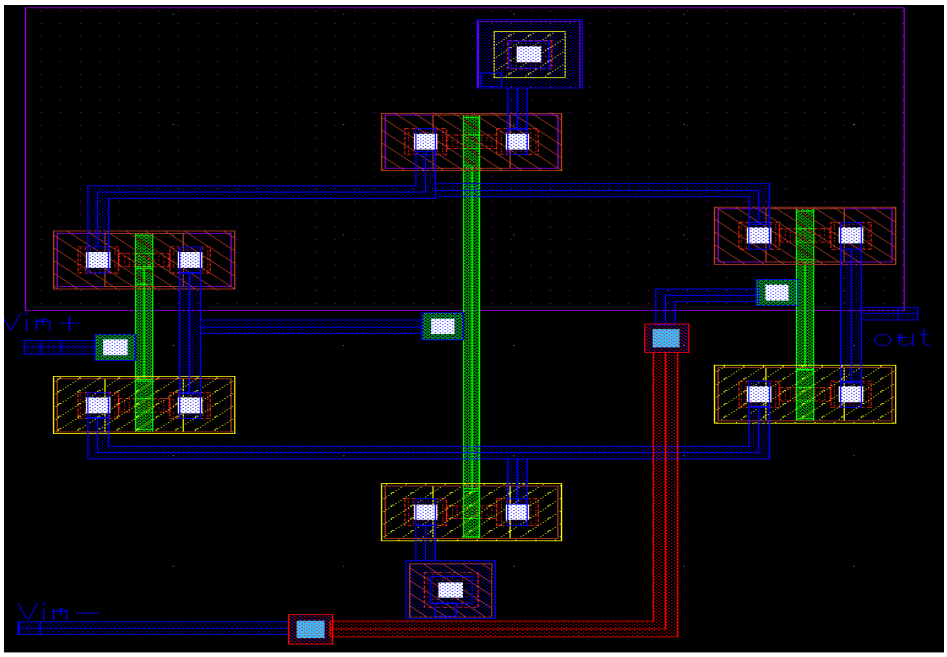


Figure 5.7 Output Buffer Layout

5.2.4 Comparator and Comparator Block Schematic and layout:

The schematic of comparator block is shown in figure 5.8.

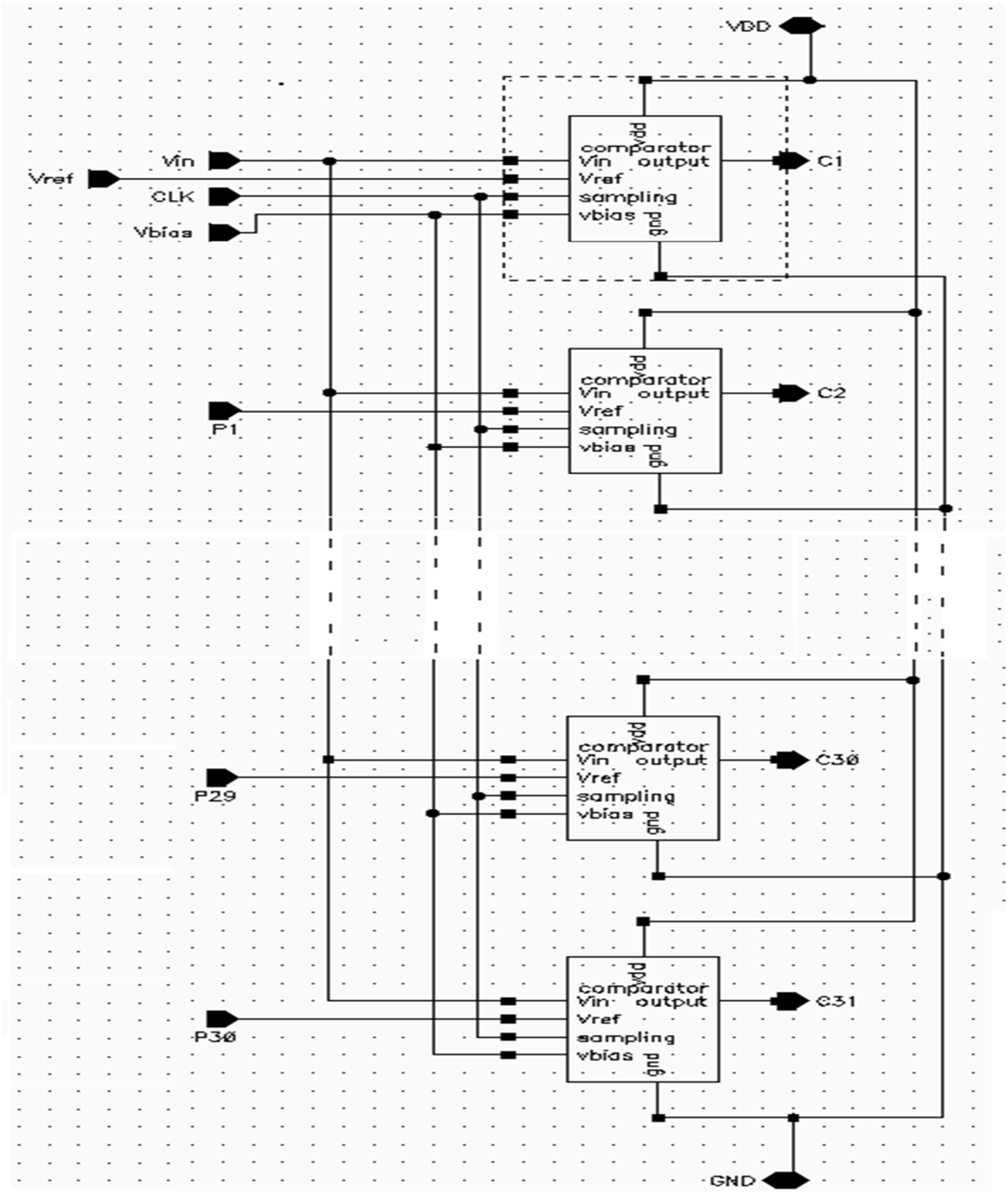


Figure 5.8 Schematic of Comparator Block

The layout of the Dynamic Latched Comparator is shown in figure 5.9.

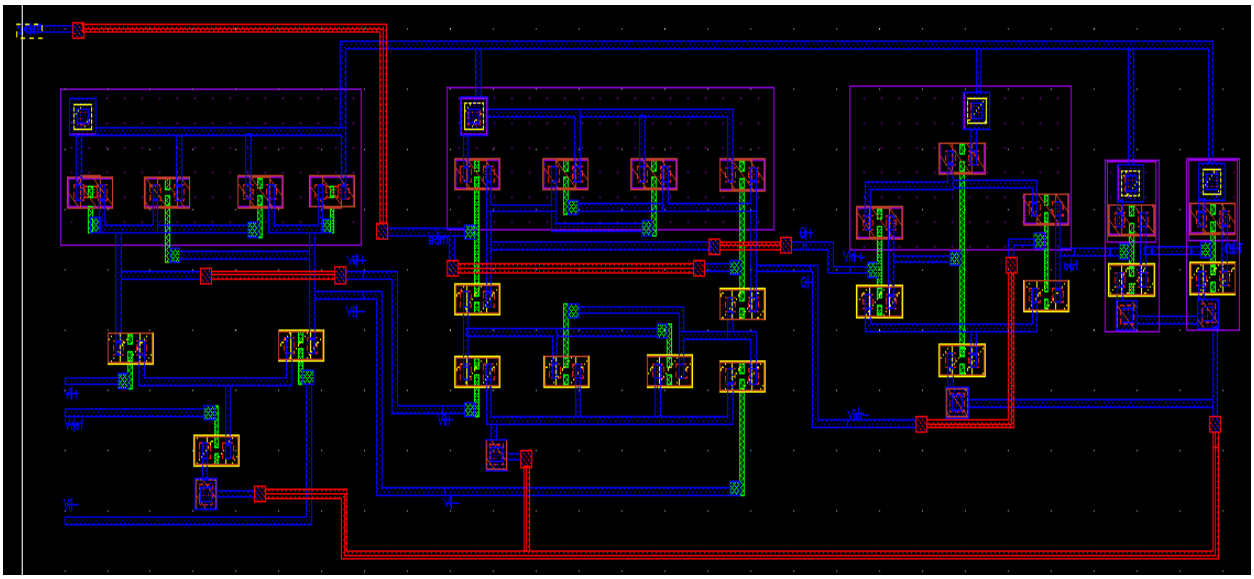


Figure 5.9 Layout of the Dynamic Latched Comparator

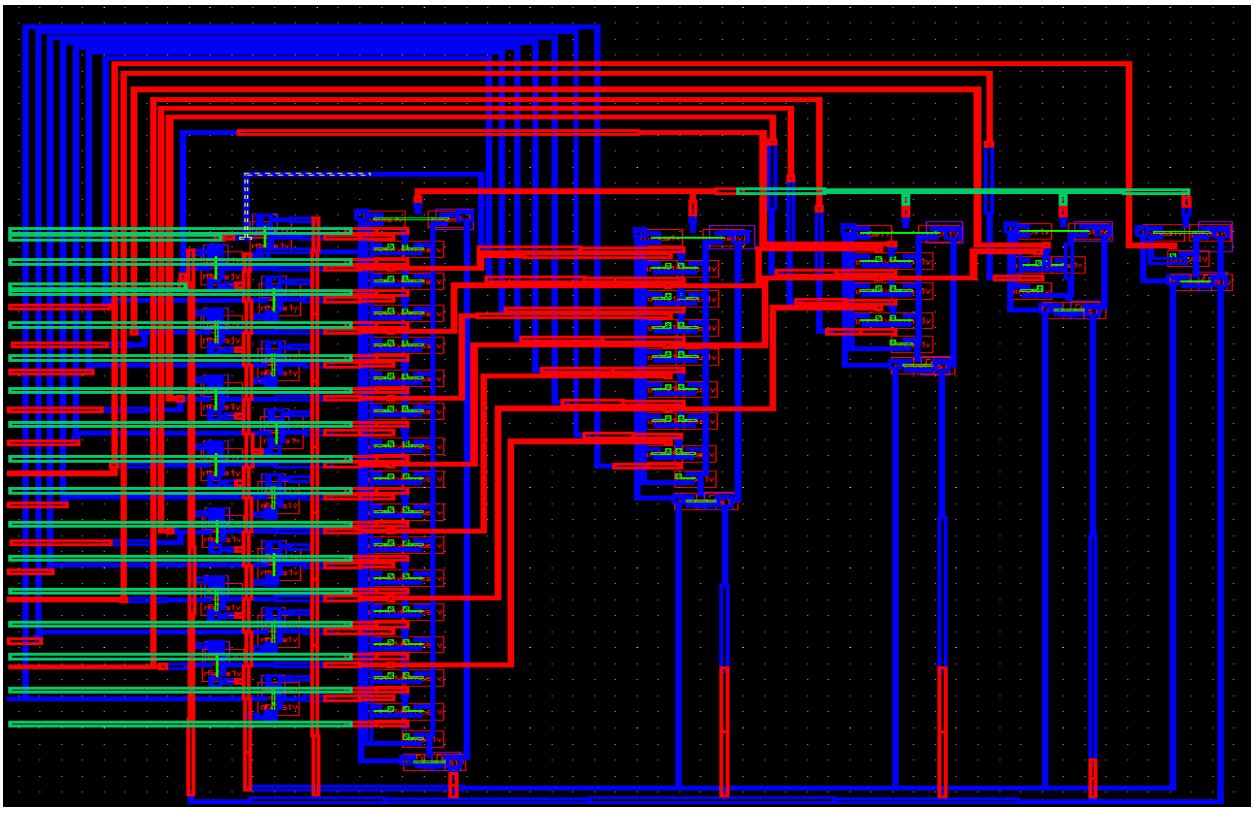


Figure 5.10 av_extracted of the encoder

The layout of comparator block is shown in figure 5.10.

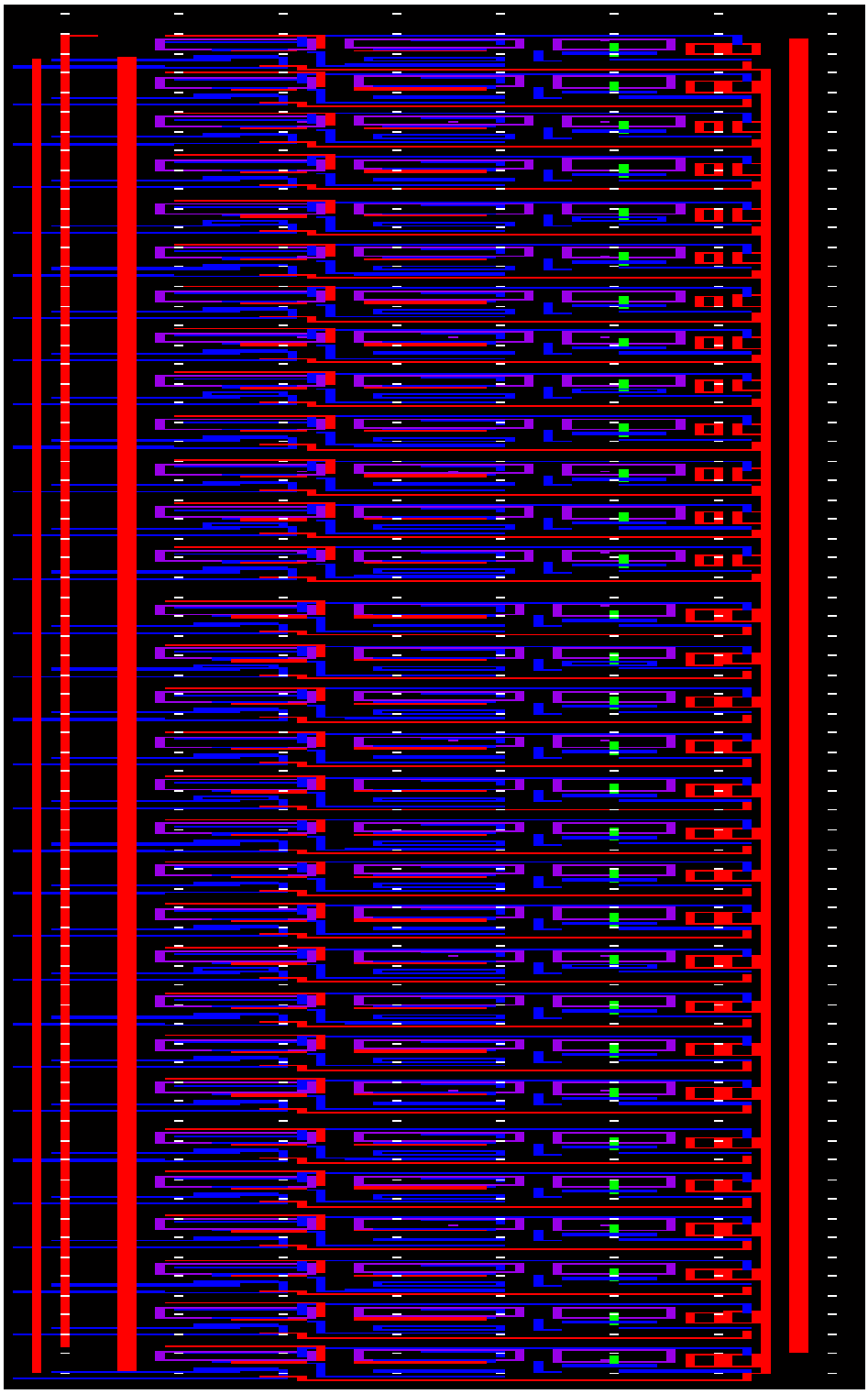


Figure 5.10 Layout of the Comparator Block

5.2.5 Outputs of Comparator Block:

5.2.5.1 DC response of the comparator:

The DC response plot is drawn between input and output. Here we vary the input signal from 0V to 1.8V.

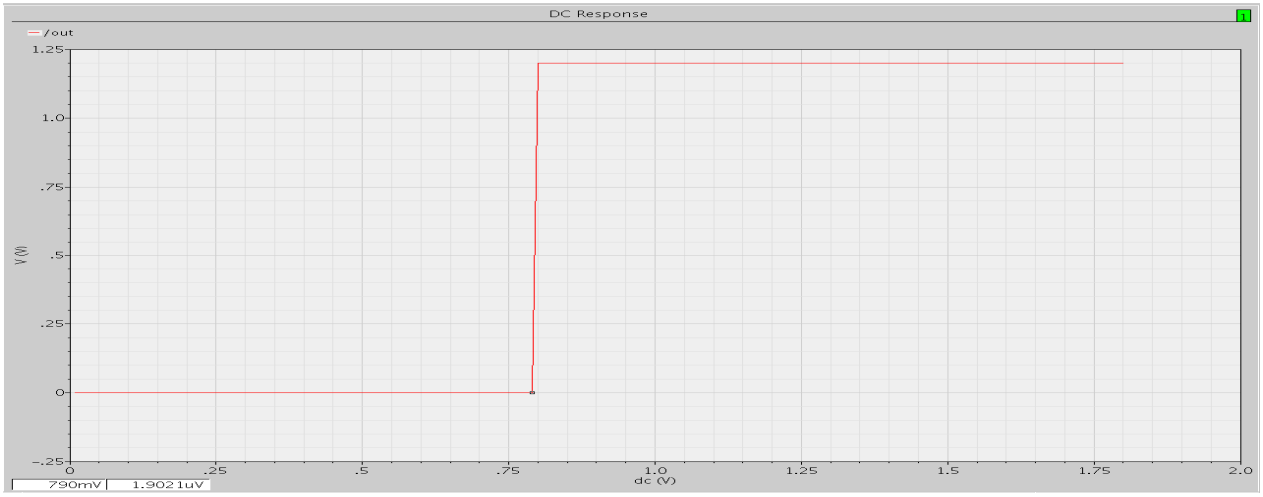


Figure 5.11 Voltage Transfer Characteristics (VTC) of the comparator

The transient response of the different latched comparator is shown below.

5.2.5.2 Transient response of the Comparator:

1. Static Latched Comparator:

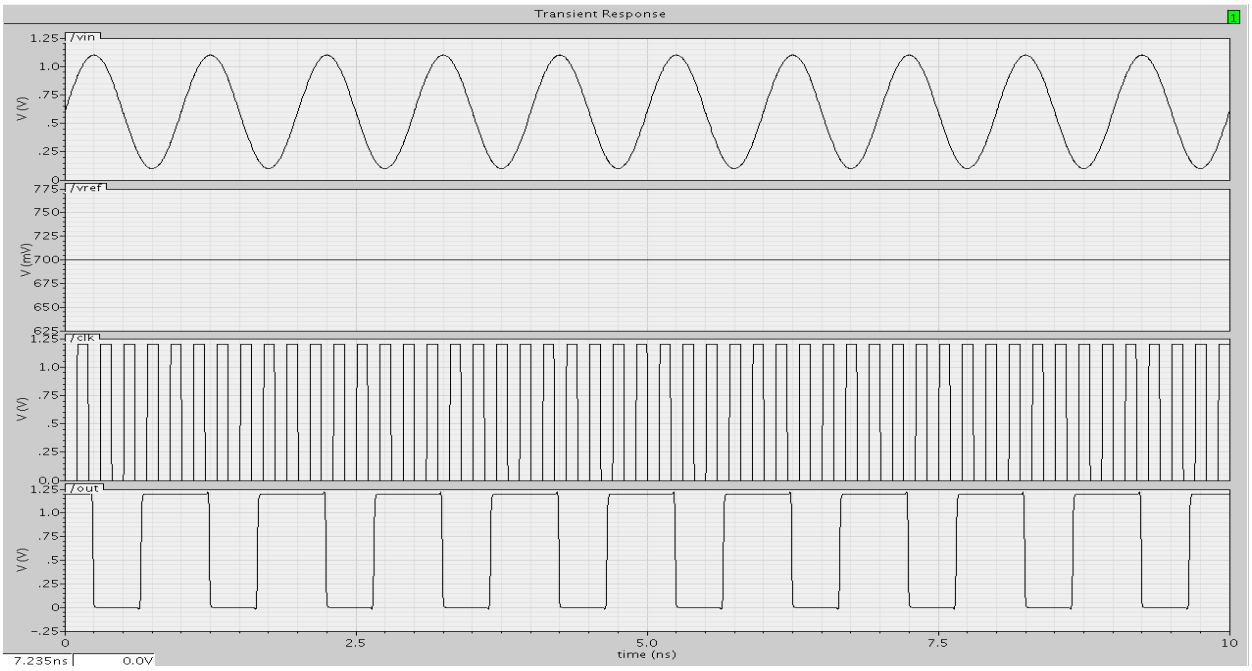


Figure 5.12 Transient response of the static latched comparator

2. Semi-Dynamic latched Comparator:

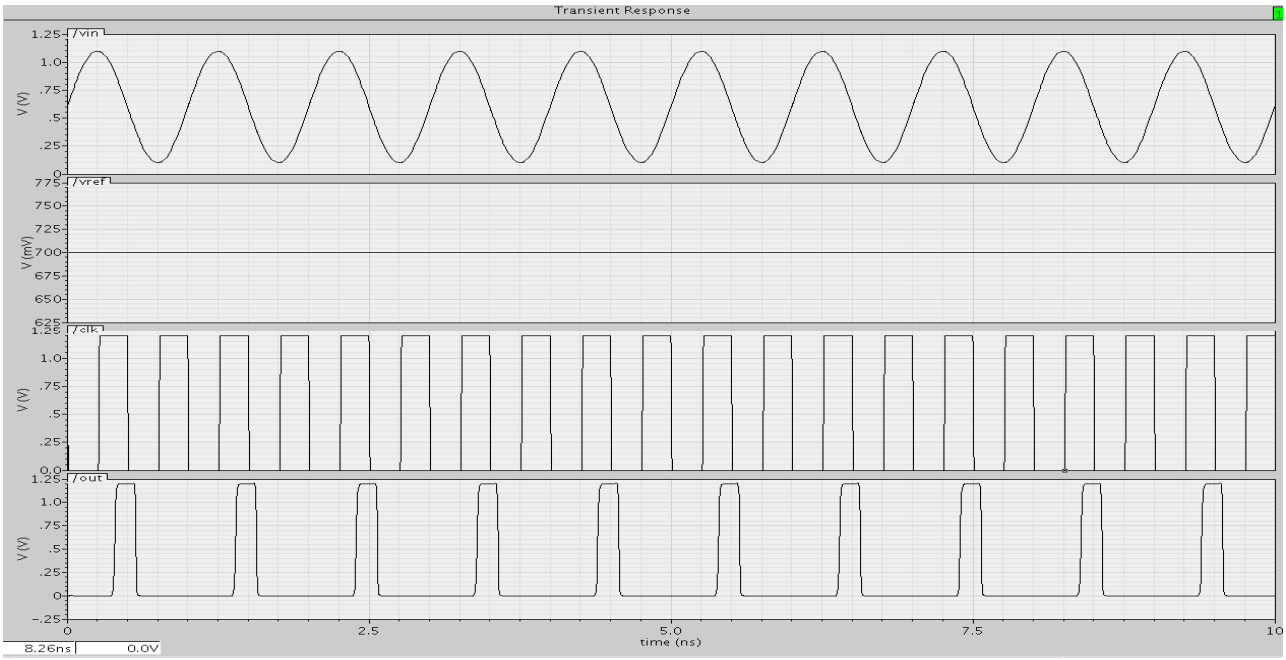


Figure 5.13 Transient response of the semi-dynamic latched comparator

3. Dynamic Latched Comparator:

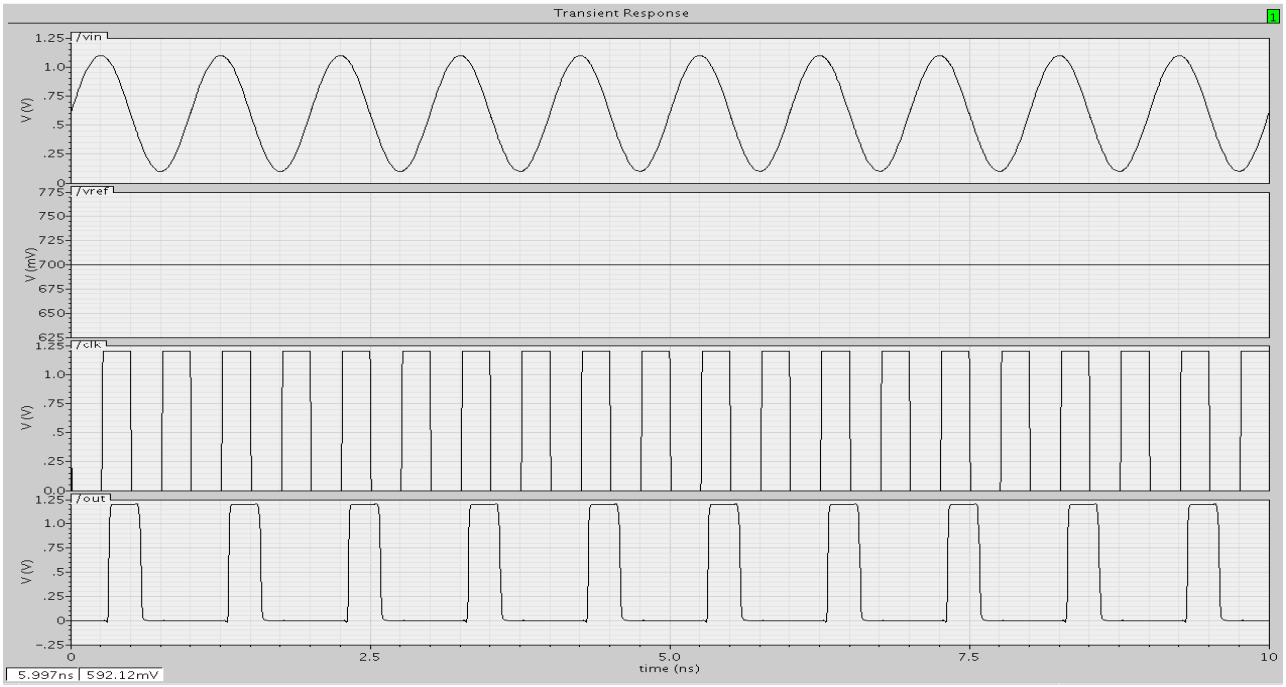


Figure 5.14 Transient response of the dynamic latch comparator

The Voltage Transfer Characteristics (VTC) of the comparator is shown in figure 5.11. The transient response of the dynamic latch comparator is shown in figure 16. The comparison of different type of comparator architecture is shown in table 5.1.

Table 5.1 Comparison and Summary of the Different Latched Comparator

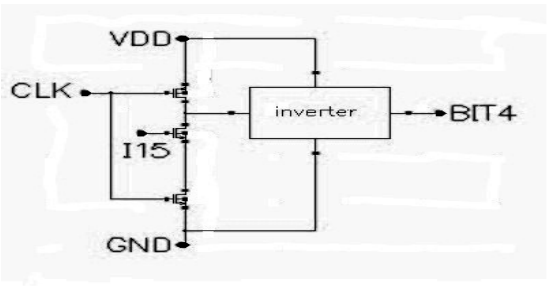
	Static Latched Comparator	**Semi Dynamic Latched Comparator**	**Dynamic Latched Comparator**
Supply Voltage	1.2V	1.2V	1.2V
Power dissipation	135.1µW	73.83µW	69.09µW
Current dissipation	112.6µA	61.52µA	57.58µA
Sampling frequency	5GHz	5GHz	5GHz
Speed	Very Fast	Medium	Slow
Advantages	Active pull-up and Pull-down →full CMOS logic levels. Zero DC current after full regeneration	Zero DC current after full regeneration.	Zero DC current in reset mode. Q^+ and Q^- are both precharged to "0". Full logic level after Regeneration stability.
Disadvantages	Q^+ and Q^- are not well defined in reset mode (Φ= 1). Large short circuit current flow in reset mode. Very noisy.	Diode divider disabled in reset mode →less short-circuit current. Pull-up not as fast. Q^+ and Q^- are not well defined in reset mode (Φ= 1). Still very noisy	The speed of dynamic latched comparator is less.

So for the better stability of the latched comparator used is the dynamic latched comparator because of stability of Q^+ and Q^- are also defined in reset mode also (precharged to "0"). As compared to the static and semi dynamic latched comparator the output in reset mode is not stable. The major disadvantage of dynamic latched comparator is speed which is less among all other latched comparator. So there is a compromise between stability and the speed. So for better stability of the latched comparator we use the dynamic latch in the latched comparator circuit.

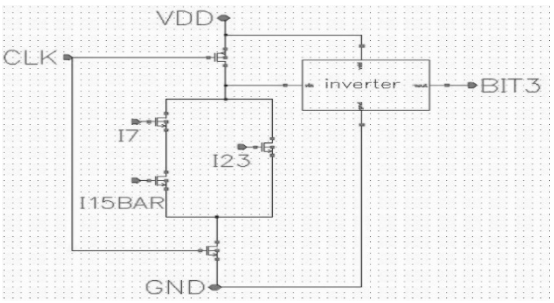
5.3 Encoder Block:

By the help of logic equations we can make the encoder circuit using dynamic CMOS logic. The circuits are separately shown in Figure 4.18:

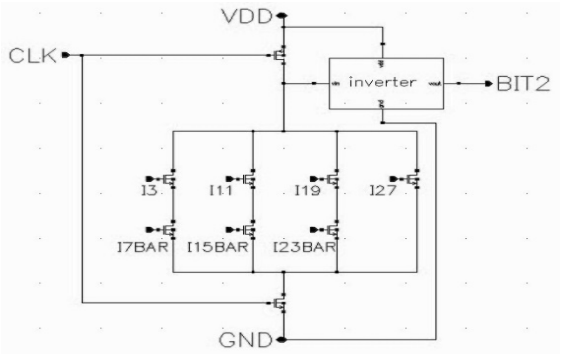
5.3.1 Encoder Block Schematic:



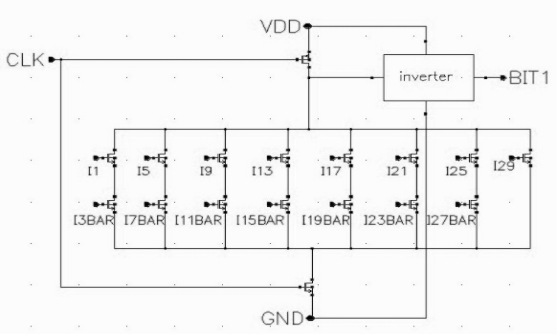
(a) Binary Code Bit 4 Generation Circuit



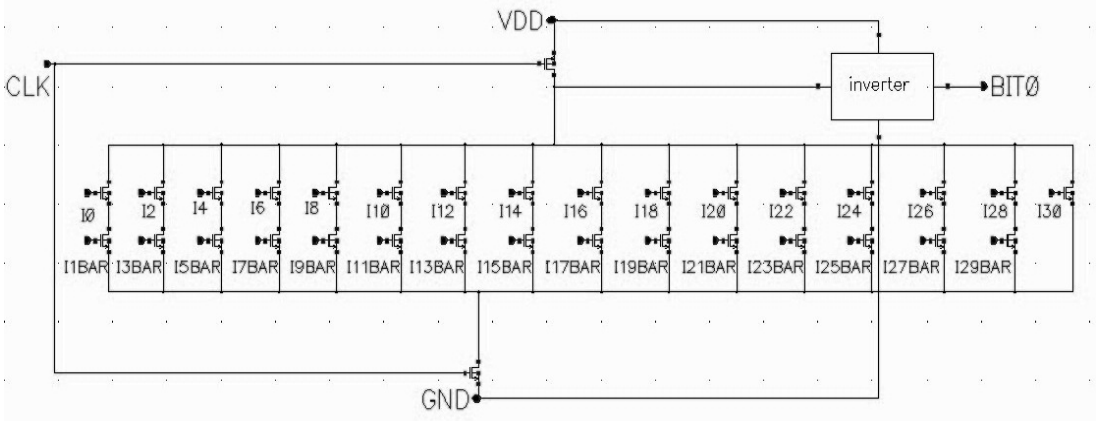
(b) Binary Code Bit3 Generation Circuit



(c) Binary Code Bit2 Generation Circuit



(d) Binary Code Bit 1 Generation Circuit



(e) Binary Code Bit 0 Generation Circuit

Figure 5.15 Schematic of Binary Code Encoder using Dynamic CMOS Logic

The encoder circuit is shown in the figure 5.8.

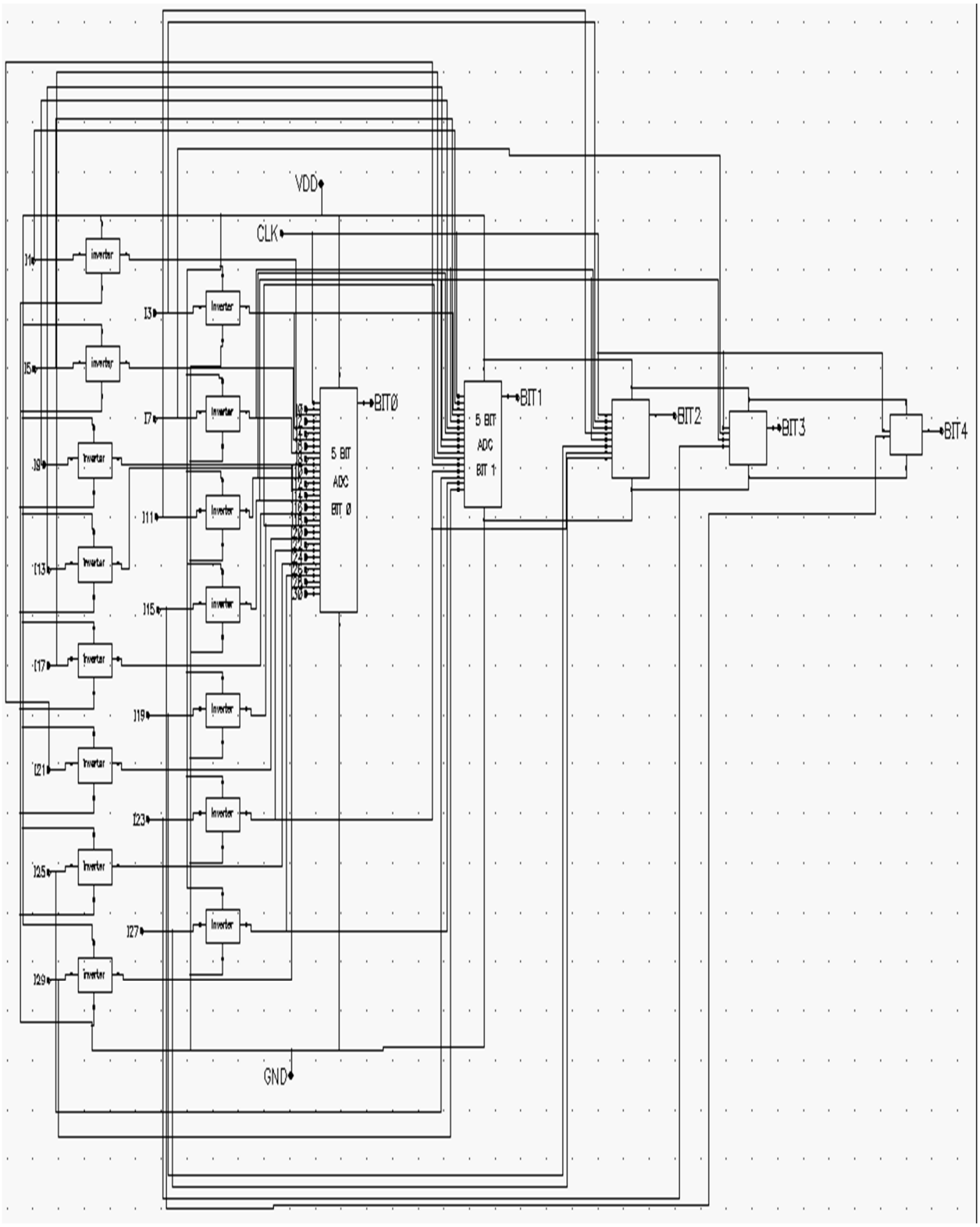


Figure 5.16 Thermometer to Binary Code Encoder

5.3.2 Encoder Block Output:

The output of the encoder is shown in the figure 5.17. There are also one comparison table 5.2. The comparison is done with the reference paper [4]. In this paper author use the pseudo dynamic logic but the power dissipation is more as shown in table 5.2. So for the concern of the power consumption we choose the dynamic logic style and the result show that the power dissipation is less compared to the reference paper. The result show the encoder power dissipation is 1.833 µW.

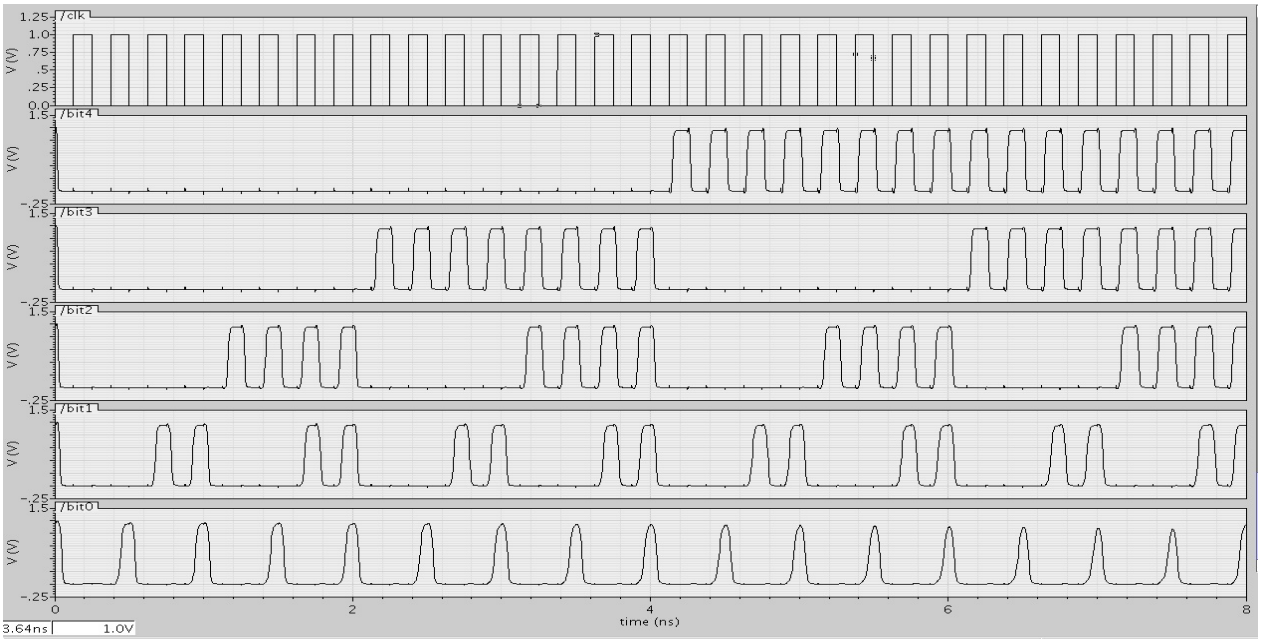


Figure 5.17 Output of the Proposed Encoder

Table 5.2 Summary and Comparison table for the proposed encoder

Results	Pseudo dynamic Encoder[4]	Proposed Encoder
Architecture	Flash	Flash
Resolution	4 bits	5 bits
Technology	90 nm	90 nm
Sampling Frequency	5GHz	4 GHz
VDD	1.2V	1.2 V
Current	154 µA	1.5275 µA
Power Dissipation	184.8 µW	1.833 µW

5.3.3 Encoder Block Layout:

The encoder layout is shown in figure 5.9.

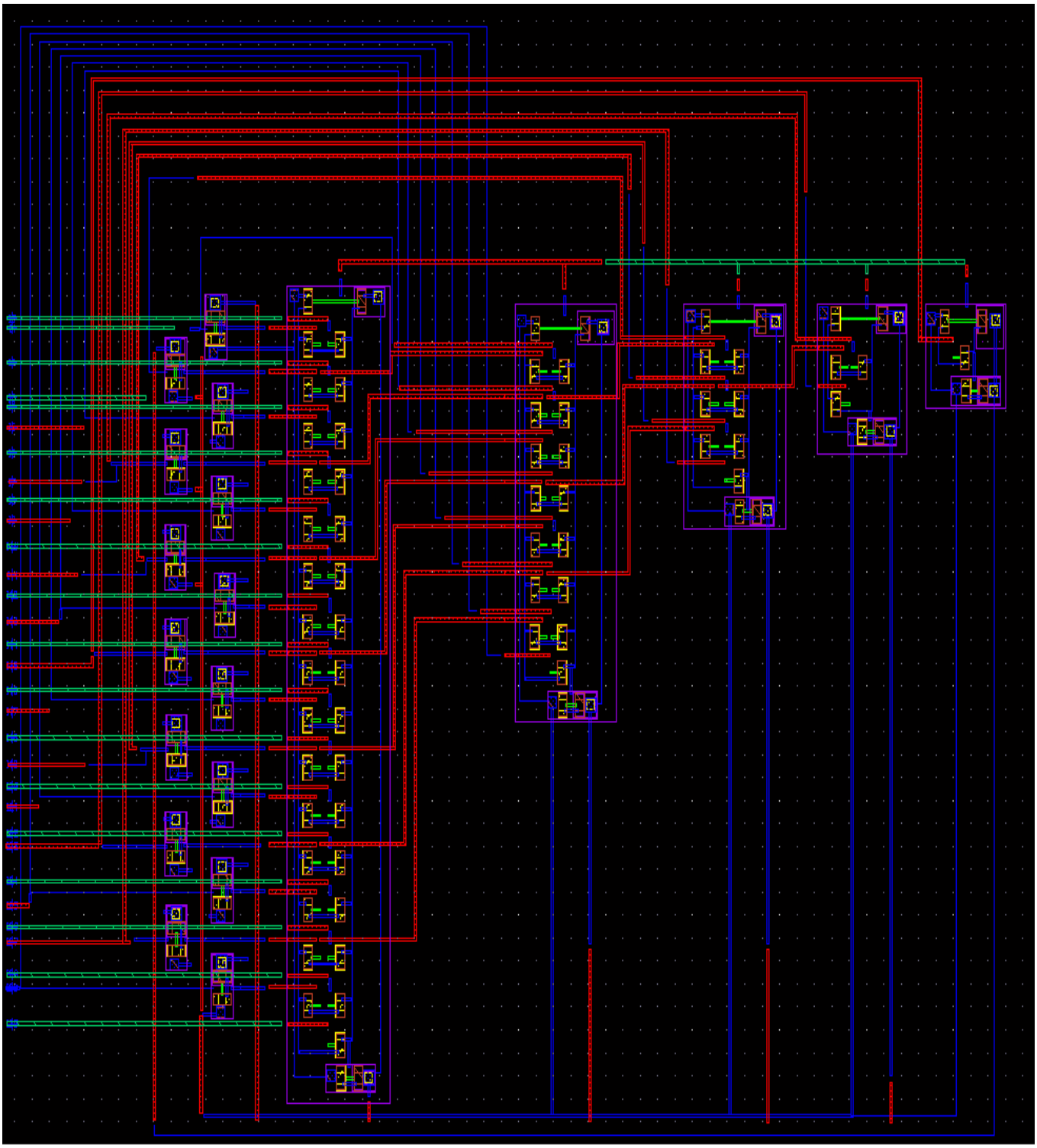


Figure 5.18 Thermometer to Binary Code Encoder Layout

CHAPTER 6

CONCLUSION AND FUTURE WORK

Conclusion and Future Work

The power dissipation of an encoder plays a major role in the design of flash ADC. The proposed encoder uses a dynamic CMOS logic to reduce the power dissipation by eliminating the presence of static power dissipation. The encoder is designed and tested using all the input combinations from the truth table and verified. The encoder is designed and simulated using gpdk 90 nm technology using CADENCE tool. In most of the 5 bit flash ADCs in 90 nm technology, the power dissipation is more as compared to other with better speed. The proposed encoder is designed in order to minimize the power dissipation and sampling frequency is high. The proposed encoder which operates at 4 GHz consumes 1.833 µW from 1.2 V voltage source. Dynamic latch comparator has been designed in order to reduce static power dissipation. The different parts of the dynamic latch comparator like: pre-amplifier, dynamic latch, and output buffer are implemented on CADENCE tool with 1.2 V power supply. The simulation results shown for a sampling frequency of 2.5 GHz and the average power dissipation of the proposed comparator is 68 µW.

The future work of the Flash ADC is to make the

1. Design of a high speed high precision reduced size CMOS comparator.
2. Design of a High Speed Flash ADC.
3. Design of a low offset comparator.
4. Design of a Low power Flash ADC.
5. Design of an optimized FLASH ADC with low power and high speed.
6. Comparison with existing FLASH ADCs.
7. Comparison with existing comparator.

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